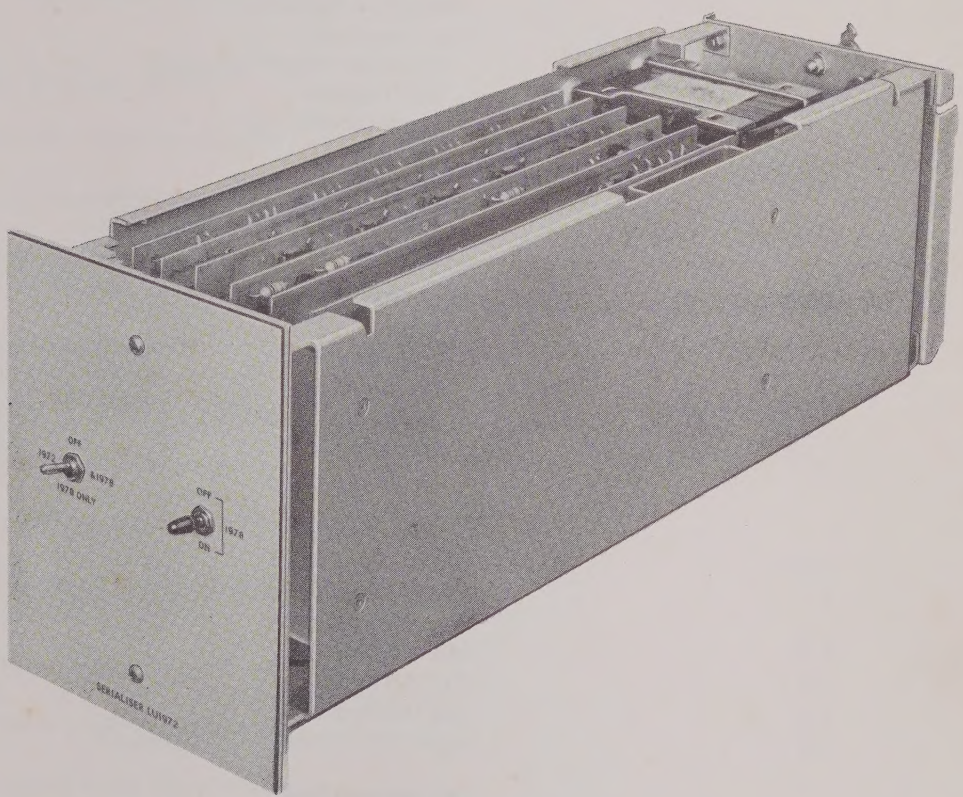
SERIALISER
LU1972



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SECTION 1
GENERAL

INTRODUCTION

The 1972 Serialiser is a quarter width rack unit for use with the Compact 'Series Two' Data Logger. It is designed to interface from the Compact Logger with low level [Integrated Circuits] input devices requiring 8 bit parallel information e.g. Facit 4070 Punch or Incremental Tape Recorder.

It may be used in conjunction with the 1978 Drive Unit for extra drive capability e.g. driving a DD110 Punch in addition to the units mentioned above.

SPECIFICATION

1. The 1972 provides low level, coded, 8 bit parallel output.
2. The output provided can be positive or negative logic.
3. Output levels from DTL stages 0V $\pm$0.75V to +3.5 to 5V.
4. Code facility is diode patched; standard provided is ASC II on a 16 x 8 matrix.
5. Word capability:-
   Word 1 - Main data word 999$\pm$99999 FC.FC.
   2 - Clock data 2359 FC.FC
   3 - Additional data [Manual Entry] 999999

N.B. "9's" indicates full BCD decode capability i.e. 0 to 15.

6. The Main data word is staticised. Clock and Additional data are not.
7. The arrangement of the character positions of the Main data word may be fully varied by wire link patching.
8. The Main data word length can be reduced from 11 characters to 4 characters.
9. Clock and Additional data words may be reduced from 6 to 4 characters.
10. Inputs for the Main data word and Clock are:-
    logical '0' = +5V to -3V
    logical '1' = -8V to -13V current required 1.5mA.
11. Inputs for Additional data word are:-
    logical '0' = +3V to +5V
    logical '1' = 0V to +1V at 1.5mA.
12. The 1972 may be used in conjunction with the 1978 and in this form may be used to drive two devices either simultaneously or one at a time.
13. The Main data word lengths for either the 1972 or 1978 may be different.
14. Command inputs:-
    Main data word Print Command A $\pm$
    Print Command B $\pm$
    Clock data $\pm$
    Additional data + only.

Temperature Range - 0^{o} to $+50^{o}$ Centigrade

Power Requirements- 95V to 130V or 190V to 260V 50-60Hz 20VA.

Weight 6lbs 2.72kg.

Dimensions - 5.25" High x 4.25" Width x 14" deep [133 x 108 x 355mm]

SECTION 2

OPERATION

GENERAL

The module can be supplied as part of a complete system or with a 1978, but is also available as a separate item.

The following information is for general reference purposes and contains all the information required to install and use it in any system.

INSTALLATION

Connector Details: Fitted to the rear panel of the module are five plugs, which carry input and output connections and mains supplies. The layout of the rear panel is shown in Figure 2.1.

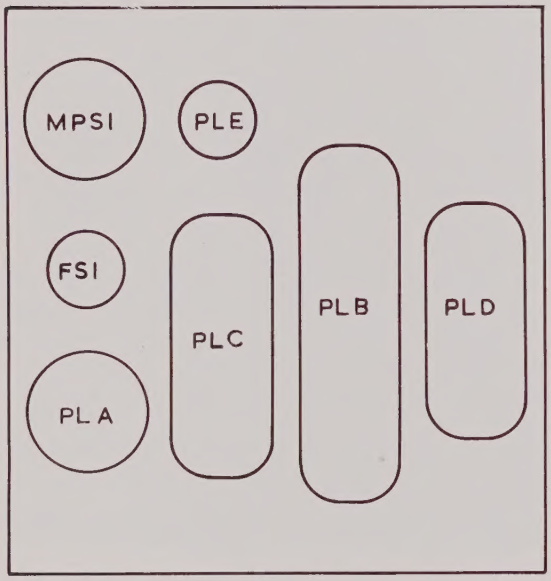


Figure 2.1. Rear Panel Layout.

Details of the plugs connections are listed in the following tables:

Pin	Service
L	LINE
N	NEUTRAL
E	EARTH

Table 2.1. Plug PLA Detail

Pin	Service
C	PRINT COMMAND 'A'
D	PRINT COMMAND 'B'
E	SYSTEM C/R

Table 2.2. Plug PLE Detail

Table 2.3. Plug PLB Detail

Pin	Service	Remarks
A	C.I. 8^3	
B	C.I. 4^3	Hundreds in
C	C.I. 2^3	8421 BCD Form
D	C.I. 1^3	
E	C.I. 8^2	
F	C.I. 4^2	Tens in 8421
H	C.I. 2^2	BCD Form
J	C.I. 1^2	
K	C.I. 8^1	
L	C.I. 4^1	Unit in
M	C.I. 2^1	8421 BCD Form
N	C.I. 1^1	
P	PRINT +ve	
R	DVM 8^4	
S	DVM 4^4	Thousands in
T	DVM 2^4	8421 BCD Form
U	DVM 1^4	
V	DVM 8^3	
W	DVM 4^3	Hundreds in
X	DVM 2^3	8421 BCD Form
Y	DVM 1^3	
Z	DVM 8^2	
a	DVM 4^2	Tens in
b	DVM 2^2	8421 BCD Form
c	DVM 1^2	
d	DVM 8^1	
e	DVM 4^1	Units in
f	DVM 2^1	8421 BCD Form
h	DVM 1^1	
j	RANGE	
k	RANGE	
m	RANGE	
n	HRS 2^2	Tens in
p	HRS 1^2	8421 BCD Form
r	HRS 8^1	
s	HRS 4^1	Units in
t	HRS 2^1	8421 BCD Form
u	HRS 1^1	
v	MINS 4^2	Tens in
w	MINS 2^2	8421 BCD Form
x	MINS 1^2	
y	MINS 8^1	
z	MINS 4^1	Units in
AA	MINS 2^1	8421 BCD Form
BB	MINS 1^1	
CC	ALARM	
DD	PRINT CMD 'A'	
EE	CLOCK CMD	
FF	CR/LF	
HH	AUTO RETURN.	To System Scanner

Table 2.4. Plug PLC Detail

Pin	Service	Remarks
A	M.E. Data 1_6	Hundred Thousands
B	M.E. Data 2_6	in 8421 BCD Form
C	M.E. Data 4_6	
D	M.E. Data 8_6	
E	M.E. Data 1_5	
F	M.E. Data 2_5	Ten thousands in
H	M.E. Data 4_5	8421 BCD Form
J	M.E. Data 8_5	
K	M.E. Data 1_4	
L	M.E. Data 2_4	Thousands in
M	M.E. Data 4_4	8421 BCD Form
N	M.E. Data 8_4	
P	M.E. Data 1_3	
R	M.E. Data 2_3	Hundred in
S	M.E. Data 4_3	8421 BCD Form
T	M.E. Data 8_3	
U	M.E. Data 1_2	
V	M.E. Data 2_2	Tens in
W	M.E. Data 4_2	8421 BCD Form
X	M.E. Data 8_2	
Y	M.E. Data 1_1	
Z	M.E. Data 2_1	Units in
AA	M.E. Data 4_1	8421 BCD Form
BB	M.E. Data 8_1	
CC	CALL B	
DD	RUN B	
EE	RETURN B	
FF	1	
HH	2	1978 DATA
JJ	4	
KK	8	
LL	C/R	COMMON RAIL
MM	M.E. COMMAND	From 1960
NN	RESET	

Table 2.5. Plug PLD Detail

Pin	Service	Remarks
A	0	Channel 0
B	1	Channel 1
C	2	Channel 2
D	3	Channel 3
E	4 (Positive Output)	Channel 4
F	5	Channel 5
H	6	Channel 6
J	7	Channel 7
K	$\overline{0}$	Channel 0
L	$\overline{1}$	Channel 1
M	$\overline{2}$	Channel 2
N	$\overline{3}$	Channel 3
P	$\overline{4}$ (Negative Output)	Channel 4
R	$\overline{5}$	Channel 5
S	$\overline{6}$	Channel 6
T	$\overline{7}$	Channel 7
U	PRINT INSTRUCTION	
V	PRINT READY	
W	COMMON RAIL	

Mains Selector Plug: The Mains Selector Plug [MSP1] is engraved with 115V and 230V markings and should be adjusted so that the metal pointer at the side of the module is opposite to the marking corresponding to the user's mains supply.

Mains Fuse: Check that mains fuse [FS1] is correctly rated:

230V Supply - 1 amp
115V Supply - 2 amp

Mounting Arrangements: The Compact Logger Series 2 cabinets have been specifically designed to accommodate a number of identically sized modules of which the Serialiser is one. The modules slide into the cabinet space frame along lips on their side panels, which act as runners. They are retained by a wing nut at the rear. Interconnecting plugs and sockets are free on their loom to avoid connector alignment problems. The 1972 can also be fitted into a 1978 when additional drive capability is required.

OPERATING INSTRUCTIONS

There are only two switches on the Serialiser, a three position switch and a two position switch and they operate as follows:-

1. Both switches set to OFF:- The 1972 and 1978 are both inoperative but the Compact Logger operation is uninterrupted. This condition also resets all bistables in both units and prior to using the Serialiser both switches should be set to OFF.

2	SWA - 1972 & 1978 SWB - OFF	The 1972 only will operate.
3	SWA - 1972 & 1978 SWB - ON	Both the 1972 and 1978 will operate.
4	SWA - 1978 SWB - ON	The 1978 only will operate

MANUAL ENTRY UNIT LU1960

This is a quarter rack width module for use with Compact Logger Series II in conjunction with the LU1972 or LU1972 and LU1978.

It has a bank of 6 edgewise switches, B.C.D. coded, each marked 0 to 15. These switches allow for setting up of data including fixed characters for processing by the LU1972.

A push button switch provides the Manual Entry Command.

The length of free cable provided enables the LU1960 to be plugged into any spare position within the system frame work.

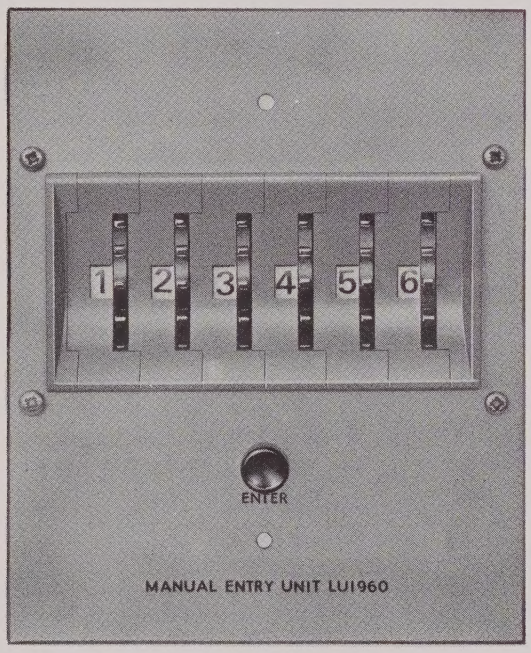


Figure 2.2 Manual Entry Unit LU 1960

Table 2.6 SKA detail

LU1960 Connector

Pin	Service
A	
B	100,000's
C	
D	
E	
F	10,000's
H	
J	
K	
L	1,000's
M	
N	
P	
R	100's
S	
T	
U	
V	10's
W	
X	
Y	
Z	UNITS
AA	
BB	
LL	Common Rail
MM	M.E. Command
NN	Reset

LINK COMBINATIONS OF LU1972

Clock, Manual Entry Non-staticised Data. Board A.

Clock Data

Consists of 4 BCD decades of time information plus two BCD decades of fixed character information.

Time Data

Fixed inputs from a 1963 Digital clock 0V to -10V switched through a 6.8K Resistor, i.e. 1½mA required at -10V.

Tens of hours decade	IC11 BCD lines 1 and 2
Units of hours decade	IC9 BCD lines 1, 2, 4 and 8
Tens of Minutes decade	IC7 BCD lines 1, 2, and 4
Units of Minutes decade	IC5 BCD lines 1, 2, 4, and 8

The above lines give time up to 2359
Maximum data out is 3979.

Clock Fixed Characters

The fixed characters on this board are patchable 0-15, by means of wire links to 0V. Each link that is patched represents a logical '1'.

FC1 (IC3)

Link P	BCD lines 1
Link N	BCD line 2
Link L	BCD line 4
Link M	BCD line 8

This position can be made a 'one out of four' line BCD decade by inserting a resistor (6.8K for 0 to -10V logic) in series with pin AJ, and prepatching the 2, 4 and 8 lines to a logic '1'

This position is prepatched to decide CARRIAGE RETURN as standard i.e. to Decode 10, links M and N are made.

FC2 (IC1)

Link K	BCD line 1
Link J	BCD line 2
Link R	BCD line 4
Link H	BCD line 8

This position can also be made a "one out of four" line BCD decade, a resistor (6.8K for 0 to -10V logic) in series with pin AA can be inserted again prepatching the 2, 4 and 8 lines.

This position is prepatched to decode LINE FEED as standard i.e. Decode 14, links J. R. H, made.

The FORMAT of clock data is determined by wire links on the Shift Register Board. These are prepatched to give the following format:-

2359 FC1, FC2

i.e. six characters called up by S6 to S11 (inclusive). This format can be changed by repositioning these links. The normal link arrangement is shown on circuit drawing 19729306.
Suppose new format is to be FC1, 2359 FC2;

This would necessitate the following link arrangement on shift register board 19729006:

Format	Link
FC1	Link S6 to pin AS
2	Link S7 to pin AH
3	Link S8 to pin AJ
5	Link S9 to pin AK
9	Link S10 to pin AR
FC2	Link S11 to pin 38

Shortened Clock Word
The CLOCK WORD can be shortened from the standard six character to a five or a four character word. e.g. clock word required 2359.

This requires that the clock start point be shortened from a six to a four character word i.e. link C-P8 be made instead of C-P6 on board F and the following links be made on board F.

Format	Link
2	Link S8 to Pin AH
3	Link S9 to Pin AJ
5	Link S10 to Pin AK
9	Link S4 to Pin AR
	Link S6 to Pin AS] See note 1
	Link S7 to Pin 38]

Note
It is important to link the last two positions S6, S7, as shown, to ensure that the FC1, FC2 data gates are closed. i.e. There must always be six links made.

Manual Entry Data
Consists of 6 BCD decades, which are able to accept information from an external source (normally from 1960 Manual Entry Unit) and enter it onto the internal Highway.

Standard Inputs
Normally required to accept I.C. levels (+5V = "0", 0V = "1") from the 1960 Manual Entry Unit. i.e. 0V input indicates bit present i.e. Most significant decade is IC12.

Link	Function	Input	
LK A/1	Represents BCD 1	0V	
LK A/2	Represents BCD 2	+5V	Decodes '13'
LK A/4	Represents BCD 4	0V	
LK A/8	Represents BCD 8	0V	

Other Inputs
These six decades will accept other input levels providing suitable input resistors are inserted in place of the wire links e.g. Input current requirements 1½mA at -10V.

Format and Shortened M.E. Word
The procedure for varying the format and for shortening the length of the M.E. word is exactly the same as the Clock Data.
Note... By changing the Format/length of either Clock or M.E. data the other is automatically changed.
i.e. if the Clock Word is shortened to a four character word then M.E. will also be a four character word.

Data 1. Board B.

Consists of:
(a) 3 staticised 4 line input BCD decades for channel identity.
(b) 1 staticised 1 line input BCD decade for polarity
(c) 1 staticised 1 line input BCD decade for FC1
(d) 1 staticised 1 line input BCD decade for FC2

Each channel identity input is buffered and sets a bistable which in turn releases the data onto the internal highway, via a controlled buffer gate.

Polarity
Decode of 12 means +ve
Decode of 13 means -ve

Print +ve Input
PLB pin p, this is the standard input
0V indicates -ve Polarity decode is 13.
-12V indicates +ve Polarity, decode is 12

Link A only used (IC6)

Print -ve Input.
Connect pin A of PLE to pin 21 of board B (19729002)
0V indicates +ve polarity, decode is 13
-12V indicates -ve Polarity, decode is 12.

Here links B and C are used (IC6).

The two fixed character inputs can be driven either as individual single lines i.e. ALARM/NON ALARM line drives FC1 and NL line drives FC2, or the NL line can drive both FC1 and FC2, so that when a NEW LINE (NL) signal is received FC1 changes to CARRIAGE RETURN and FC2 changes to LINE FEED.

Single Line Characteristic

FC1 Link D used as standard ($1\frac{1}{2}$mA at -12V)
Input 0V indicates NON-ALARM, decode 11 = Space
Input -12V indicates ALARM, decode 10 = Carriage Return
The inverse can be obtained simply by connecting the input with links E and F made instead. Here the input must be capable of supplying 3mA at -12V.

FC2 Link H used as standard.
Input 0V indicates NO LINE FEED decode 15 = Space
Input -12V indicates LINE FEED decode 14 = LINE FEED
Again if Links K and J are used the inverse inputs can be used. (3mA required at -12V)

Single line control of FC1 and FC2
LINKS L, H, F and E connected.
Here FC1 follows FC2 input i.e. when a line feed is called a Carriage Return is inserted so that Carriage Return and Line Feed is punched out.

Input to FC2 = 0V	FC1 decodes 11 Space
	FC2 decodes 15 Space
Input to FC2 = -12V	FC1 decodes 10 Carriage Return
	FC2 decodes 14 Line Feed

In the above configuration the alarm/non alarm input is ignored. The reverse of the above can also be achieved i.e. FC1 can drive FC1 and FC2.

LINKS L, D, K and J connected

Input to FC1 = 0V	FC1 decodes 11 Space
	FC2 decodes 15 Space
Input to FC1 = -12V	FC1 decodes 10 Carriage Return
	FC2 decodes 14 Line Feed

In the above case the Line Feed input is ignored.

Data 2. Board C.

Consists of 5 staticised 4 line input BCD decades for DVM and Range information. The 8^4 input to the range decade is brought out to a pin connection but is not normally used.

There are no link connections on this board.

Logic Board. Board D.

Print Command Inputs both +ve and -ve inputs are provided. Print Command 'A' Input on PLB pin DD
+ ve input Link B used. (Standard CL2 input)
-ve input Link A used.
The Print Command 'A' input is from PLB pin DD input, hence it follows the normal CL2 upper or lower position drive rules.
i.e. 1972 plugged into Upper position Print Command A is RTN/AL input. Lower position Print Command A is RTN only input.

Print Command B

The Print Command B can "pick up" either the RTN/AL or RTN ONLY input regardless of the position the 1972 is plugged in.

RTN/AL input required.	Link C used
RTN ONLY input required	Link D used (Standard input)
+ve input required	Link H used (standard input)
-ve input required	Link J used

Print Command Clock

-ve input Link E used (Standard input)
+ve input Links F and G used

Manual Entry Command

This input must be a positive going 5V edge, standard input is 0 to +5V.

Run A, Run B, Commands

When the 1972 is used with 1978 two output devices can be driven simultaneously, one from the 1972 and one from the 1978. Because of this dual capability the logic controls are distinguished by "A" and "B" suffixes. The 'A' lines normally drive board (19729005) while the 'B' control lines are fed out to the 1978 drive board.

The Run A and Run B signals are normally patched up to drive their own respective drive boards i.e. Link L and Link K are used.

Print Cmd. Input	Link Used	Start Point of Word	
Print Cmd. 'A'	Link L	Data Start A link	(Standard form) 1972 as a Single Drive Unit
Print Cmd. 'A'	Links L and M	Data Start A link	1972 and 1978 using the Print command A input
Print Cmd. 'B'	Link K	Data Start B link and SX	Provides Separate start point for B Drive Unit

Auto Return
The Auto Return line can be used either in a staticised or non-staticised mode.

Staticised mode STAT link made. (Standard form)

The 1972 will generate an Auto Return as soon as the data has been written into the 1972 staticisor. The period of the Auto Return pulse is variable but is normally set for approximately 3mS. When used with other CL2 drive units the Auto Return period must be extended until these units have clamped to -10V. The period is easily varied by changing the timing capacitor C16 on board 19729004

A non-staticised Auto Return pulse is available which is triggered at the end of the word, i.e. off the last position of the Shift Register. Here the NON-STAT link is used.

Decode/Encode Drive. Board E

Code
The 1972 is provided with ASC II/ISO7 code with all diodes on the parity line patched in. For even or odd parity the relevant diodes can be cut out.

Code Output Control
The timer period in which the coded data is presented at the output can be varied according to Link A and Link B connections.

Link A The data is presented to the output lines for the full print-out period required by the output device. This data is removed by a sync pulse back from the machine when it has finished its print-out cycle.

Link B The data is presented for the time period determined by the Punch Instruction monostable. This period is nominally set for 3mS but can be changed to suit the output machines requirements.

Synchronization Requirements
Links C, D, E, F, H, J, are available for varying feedback signals received from output peripherals.

Link C This link is connected as standard for Facit 4070 punch. The input PUNCH READY must normally be +5V at rest, clamped to 0V while the output peripheral is busy and then released to +5V when it is ready to accept new data.

Link D Used for feedback signals of the reverse polarity in the above. i.e. 0V at Reset, going to +5V while busy and then clamping to 0V again when ready to accept new Data.

Links E, F These links are provided to trigger a monostable either to simulate feedback pulses (for peripherals which do not provide synchronization signals) or simply as a delay before new data is presented to the output. The monostable can be triggered on either the leading (link F) or lagging (link E) edge of the Punch Instruction monostable.

Links J, H These are provided so that either output of SS2 can be used. The output of this monostable can either directly reset the Run bistable (link C connected) or the output can be shaped before resetting the Run bistable (Link D connected).

Shift Register. Board F
The data written into the 1972 staticising register is sampled in a serial mode determined by link connections on this board.

Data Start 'A' Link A to P1(up to P8 inclusive)
Determines the length of the main Data word generated by the Print Command 'A' input. Normally set for an eleven character word (Link A-P1) it can be shortened down to a four character word

Eleven character word link A-P1 made
Seven character word link A-P5 made
Four character word link A-P8 made

Data Start 'B' Link B to P(1-8)
Determines the length of the data word generated by the Print Command 'B' input. Nominally set for an eight character word (Link B-P4). This can be varied as above.

Clock/Manual Entry Start C to P (6-8)
Determines the length of the Clock/M.E. word

Link C-P6	6 character word
Link C-P7	5 character word
Link C-P8	4 character word

Variations of Format

Main Data Word

The main data word is prepatched to give the following format:-

Channel identity	999
Polarity	$\pm$
DVM	99999
Range (0-7)	99999
Fixed characters	FC1 FC2

This is achieved by inserting links so that the true shift Register positions S1 to S11, are connected to the Defined Positions D1 to D11 respectively.

Variations in format are achieved by patchine the 'D' positions to the required S positions. Two examples are shown below:

Example 1

Format required:	±	9	9	9	9	9	FC1	9	9	9	FC2
True Shift Register Positions	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
Linked to Defined Positions	D4	D5	D6	D7	D8	D9	D10	D1	D2	D3	D11

Example 2

Format required:	FC1	+ -	9	9	9	9	9	FC2	9	9	9
True Shift Register Position	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
Linked to Defined position	D10	D4	D5	D6	D7	D8	D9	D11	D1	D2	D3

Note... Even in a shortened wordlength all S-D links must be made. This includes unused inputs.

Clock/M.E. Format

The Clock/M.E. word can be changed in the same way as the main data word.

Normal format is	TIME
Clock word	2359 FC1 FC2
M.E. word	999999

The patching is achieved by linking the required Shift Register position to the appropriate edge connector pin Two examples are shown below:

Example 1

Format	2	3	5	9	FC1	FC2
Shift Register Position	S6	S7	S8	S9	S10	S11
Linked to Edge Connector Pin	AH	AJ	AK	AR	AS	38

Example 2

Format	FC1	2	3	5	9	FC2
Shift Register Position	S6	S7	S8	S9	S10	S11
Linked to Edge connector Pin	AS	AH	AJ	AK	AR	38

SX LINK

Sx is the "pick-up" shift register position for the 'B' output device, when the 1972 is used with a 1978 Dual Drive Unit.

By patching Sx to a particular Shift Register position the commands out to the 1978 are inhibited until that position is reached.

'A'	Drive Unit	999 ± 99999 FC1 FC2 output
SX	Linked to S4	
'B'	Drive Unit	± 99999 FC1 FC2 output

Hence Sx is used in conjunction with the Data Start 'B' link and they must both be linked to the same shift register position.

In the above example we have:-

Data start 'B' link is B-P4
SX pick-up link is SX - S4

SECTION 3

TECHNICAL DESCRIPTION

PRINCIPLES OF OPERATION

The 1972 Serialiser receives information from the Compact Logger including the Digital Voltmeter [DVM] and Clock or in some cases Manual Entry. All inputs are fed via a series of gates, each decade in turn placing B.C.D. information on a 4 bit Highway. This Highway information is then converted to decimal and, via a matrix board, a predetermined code is presented in 8 bit parallel form for the output device in use.

A maximum of 11 characters is available for the Main data word as follows:-

$$999\pm99999\ FC.FC.$$

The normal arrangement for the Compact Logger being:-

999 - Channel Identity
$\pm$9999 - DVM polarity and reading
9 - Range
FC.FC. - Fixed Characters.

The 11 character Main data word may be shortened from 11 to a 4 character word, the 4 characters being any combination and the Main data word selected by wire links.

Each character decodes from an 8421 BCD input in turn as serialisation through the Shift Register occurs from S1 to S11. Polarity and fixed characters differ in that a 1 or $\overline{1}$ is detected at the input.

LOGIC DESCRIPTION

Staticisor Logic

Reference: Logic Diagram 19727002

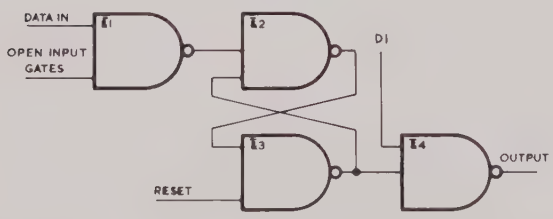


Figure 3.1 Staticisor Logic

Reset State:- OPEN INPUT GATES is normally logical 1 [low] in this state, thus the output of NAND gate $\overline{\&1}$ is logical 0 [high]. When the RESET line goes to a logical 1 [derived from the Serialiser Logic Board] the output of $\overline{\&3}$ is forced to logical 0, as both inputs to $\overline{\&2}$ are logical 0 its logical 1 output latches $\overline{\&3}$ output at logical 0. S1 input to $\overline{\&4}$ is at logical 1 therefore the output of $\overline{\&4}$ is logical 0. This is the reset state of the Staticisor.

When OPEN INPUT GATES goes to logical 0, $\overline{\&}$ 1 is primed such that its output will depend on the Data input.

Data Inputs:- A logical 0 input will produce a logical 0 output to the highway.

A logical 0 input sets $\overline{\&1}$ for a logical 1 output, $\overline{\&2}$'s output is thus logical 0 forcing $\overline{\&3}$ output to logical 1 which latches $\overline{\&2}$'s output at logical 0 such that variations of $\overline{\&1}$ output will not offect the Staticisor output. $\overline{\&3}$'s logical 1 output gives a logical 0 output from $\overline{\&4}$ to the highway and S1 going to logical 0 will not alter this output.

A logical 1 input will produce a logical 1 output to the highway.

A logical 1 input gives a logical 0 output from $\overline{\&1}$, $\overline{\&2}$'s output goes to logical 1 forcing $\overline{\&3}$ output to logical 0 which latches $\overline{\&2}$'s output at logical 1. $\overline{\&3}$'s output being logical 0 primes $\overline{\&4}$ such that when S1 goes to logical 0 the output to the highway is a logical 1.

The action of all staticisors is identical, the outputs being fed onto the internal highway and via four pairs of NAND gates to the external highway. The information is released to the external highway by a DATA 1 input to NAND gates $\overline{\&77}$, $\overline{\&78}$, $\overline{\&79}$, $\overline{\&80}$, $\overline{\&102}$, $\overline{\&124}$, $\overline{\&146}$ and $\overline{\&168}$. The DATA 1 input is derived on the Serialiser Logic Board and is high during a Print cycle.

D4, D10 and D11 differ from the rest of the staticisors in that only the '1 bit' is variable, the other lines to the internal highway being fixed. The '1 bit' stage is identical to the previous staticisors, the 2, 4 and 8 bits being set as follows:-

D4 to give 12 [variable 1 bit allows 12 or 13]
D10 to give 10 [variable 1 bit allows 10 or 11]
D11 to give 14 [variable 1 bit allows 14 or 15].

Clock and Manual Entry Logic

Clock Data Logic

A maximum of 6 characters is available for clock information allowing for a count of 2359 FC.FC. controlled by the Shift Register positions S6 to S11.

The tens of hours section has a count of 1 and 2. the 8 and 4 bits being wired to produce 'no bit' present outputs. Similarly the tens of minutes is set as the maximum count normally required is 5.

M1 going to logic O primes NAND gates $\overline{\&}1$, $\overline{\&}2$, $\overline{\&}3$ and $\overline{\&}4$. The Clock inputs to pin F and J will be logical 1 or 0 depending on the information and the NAND gate output will be logical 0 or 1 respectively. [1 indicates bit present.] All stages are identical and as serialisation through the M positions occur so that next set of gates open placing clock information on the internal highway. This information is fed to NAND gates $\overline{\&}49$, $\overline{\&}50$, $\overline{\&}51$ and $\overline{\&}52$ where it is released when a CLOCK GATE pulse goes to a logical 0 [produced on Serialiser Logic Board].

It should be noted that there is no staticisation on Clock information.

Manual Entry Logic

A maximum count of 999999 is available and the operation is identical to Clock Data Logic. The information is released to the external highway when MANUAL ENTRY GATES goes high. Again there is no staticisation.

The Standard input for Manual Entry information is 0V to +5V from the LU1960, Manual Entry Unit.

Shift Register

This board contains 12 J-K Bistable packages.

The Data Zero input resets all bistables prior to commencing a print out.

A DATA START input will set the first I.C., [depending on the Link position] and when one character has been printed a STEP ON pulse clocks the Shift Register to the next position.

The links on the Q outputs of the bistables allows the S positions to be called in any order required. This enables both MAIN DATA WORD, and CLOCK/ MANUAL ENTRY DATA WORD to have a varied format.

Control Board Logic

Reference: Serialiser Command Logic Diagram 19727001.

Print Command A

The Print Command input may be negative or positive, and via one or two inverters [selected by links] produces a logic 1 set input to FFA1. ZERO input is normally logical 0 [high], thus the logical 1 set from the inverter produces a logical 0 Q output. As all other inputs to $\overline{\&}1$ are normally logical 0, the logical 0 Q produces a logical 1 output from $\overline{\&}1$ which sets FFA2 for a logical 0 Q output, priming $\overline{\&}5$ and, via $\overline{O}1$ and I13, a logical 0 is fed to I19 and A1. $\overline{O}1$'s logical 0 output is fed back to $\overline{\&}1$, $\overline{\&}2$, $\overline{\&}3$ and $\overline{\&}4$ inhibiting them so that a further Print Command will not affect the second set of bistables. I19 output [DATA ZERO AND RESET STATES] clears the Shift Register and all staticisors. The output of A1 is delayed and after the system has been reset a logical 0 is fed to $\overline{\&}5$, Q is already logical 0 thus a logical 1 DATA START A pulse initiates the sequencing of the Shift Register. A1 output via I17 produces a logical 1 output which resets bistables FFA1, FFB1, FFME1 and FFC1. This logical 1 is also fed to I18 to give a logical 0 OPEN INPUT GATES which allows all staticisors to be set according to their inputs. FFA2 $\overline{Q}$ output, now logical 1, inhibits $\overline{\&}6$ to produce a logical 0 DATA 1 pulse which allows the release of information from the MAIN DATA WORD to the external highway as the S Register sequence gates it.

An AUTO RETURN pulse, due to A1 output, will be fed to the Scanner unit and a full explanation of the logic is detailed later.

A1 output via I16 gives a RUN A pulse which is fed to FF RUN on the Decode/Encode Board. CALL A is logical 0, due to $\overline{O}3$ being satified by a logical 1 $\overline{Q}$ from FFA2.

FF RUN, due to CALL A being at logical 0 and RUN A at logical 1 sets $\overline{Q}$ to logical 0. $\overline{\&}13$ is satisfied and sets SSM1 to give a PUNCH INSTRUCTION. When the information has been punched a PUNCH READY pulse [External input or due to SSM 2] produces a negative edge through a pulse gate [I12 and $\overline{PA1}$] to clock over FF RUN, $\overline{Q}$ now goes to a logical 1 and Q logical 0. The logical 0 Q is fed to $\overline{\&}12$ [RETURN B logical 0] and the logical 1 output via A2 produces a STEP ON pulse giving the next S position. Also via I15, DLY and PA1 a delayed pulse gives the next RUN A pulse, the delay allowing the Shift Register to STEP ON prior to a RUN A pulse.

On reaching position D11 the next STEP on pulse gives a logical 1 $\overline{S}12$ which will inhibit $\overline{\&}16$ and prevent further RUN A pulses. $\overline{S}12$ also clocks over FFA2, FFB2, FFME2 and FFC 2 to the state Q logical 1 and $\overline{Q}$ logical 0 thereby removing the inhibit from the DATA 1 gate.

Print Command B

This input allows acceptance of a further Print Command when used as a dual Serializer i.e. with a 1978 in use. It is not normally used when the

1972 is used as a plug in unit with the Compact Logger. When plugged into a 1978 however the Print Command B circuitry can be used as the Return B, Call B and Run B lines connect to a circuit similar to that of the 'A' circuit in the 1972.

Manual Entry Command

This operates in a similar manner to a Print Command 'A' [only on positive inputs].

FFME2 $\overline{Q}$ output going to logical 1 makes $\overline{O}2$ output go to logical 0 priming $\overline{\&}8$ and $\overline{\&}9$. A further output via I14 inhibits $\overline{\&}10$ preventing A1 output causing an AUTO RETURN as Manual Entry information is not staticised and must be held until print out is complete. I14 output also satisfies $\overline{O}3$ and $\overline{O}4$ giving logical 0 CALL A and B output. $\overline{\&}9$ is satisfied via $\overline{O}1$, I13 and A1 to give a logical 1 RUN B pulse, via A3, and I16 inverts A1 output for a logical 1 RUN A pulse. Thus when two output devices are used both will print out Manual Entry Information.

FFME2 Q output is logical 0 and via $\overline{O}1$, I13, A1 and $\overline{\&}9$ produces a CLOCK and M.E. START pulse which is fed to the Shift Register. Q also provides a M.E. GATE pulse releasing information to the external highway.

Manual Entry data operates from position D6 [M1] onwards, hence there is no requirement to print D1 to D5. This is achieved by I10, D6 is logical 1 until this position is reached, the input to $\overline{\&}14$ is therefore logical 0 and the logical 1 output is latched by $\overline{\&}15$. RUN B is held at logical 0 via $\overline{\&}17$. D6 going to logical 0 via I10 places a logical 1 input to $\overline{\&}14$, its output is now logical 0 'latched' again by $\overline{\&}15$ [$\overline{S}12$ input logical 0]. Print out can now commence.

The Sx input to I11 performs identical action to the D6 input, and is used only when two output devices are being driven [LU1978 in use], Sx may be wire linked to any position allowing flexibility of the start position.

Clock Data Command

This is identical to a Manual Entry Command but any Clock Information has priority. This is achieved by allowing the $\overline{Q}$ output of FFC1 to inhibit $\overline{\&}1$, $\overline{\&}2$ and $\overline{\&}3$ when clock is called [$\overline{Q}$ at logical 1].

Auto Return

There are two sources of Auto Return.

1. When FFA2 or FFB2 are set, the logical 0 Q output via $\overline{O}1$, I13 and A1 produces a logical 0 input to $\overline{\&}10$. As FFME 2 or FFC2 are not set $\overline{O}2$ is inhibited to give a logical 1 output, this is inverted by I14 to give a second logical 0 input to $\overline{\&}10$. $\overline{\&}10$'s logical 1 output to $\overline{\&}11$ produces a logical 0 input to SSM1. SSM's output is inverted by I21 to give to logical 1 AUTO RETURN. Thus an AUTO RETURN pulse has been produced only a short period after the information was received and before print out has been completed. On receipt of the trailing edge of the AUTO RETURN pulse [going positive] the Scanner Module will select the next channel and the DVM will commence producing the next reading. This is permissible as the Staticisors will remember the information for the print out period. This method of operation allows for faster print out as the period of waiting for the DVM to digitize has been eliminated.

2. If FFME2 or FFC2 are set, $\overline{Q}$ will be logical 1, $\overline{O}2$ is satisfied giving a logical 0 output which, inverted by I14 places a logical 1 input to $\overline{\&}10$. The logical 0 output of $\overline{\&}10$ therefore primes $\overline{\&}11$. When S11 goes to logical 0 $\overline{\&}8$ is satisfied and the logical 1 output produces a logical 0 output from $\overline{\&}11$ which sets SSM1, the logical 0 of which gives a logical 1 AUTO RETURN via I21. Thus for Manual Entry or Clock information it can be seen that an AUTO RETURN pulse occurs later in time than for a Print Command; this is because the Clock and Manual Entry data inputs are not staticised and information must be held until serialization through the Shift Register is completed.

Using Two Print Out Devices

When the 1972 is used with a 1978 it is able to operate two print out devices. These are controlled by RUN A and RUN B, a similar circuit to the Decode/Encode Board being contained in the 1978.

It is important when using two devices that both keep in step; commencing a print out at the same time. This is achieved as a STEP ON pulse will only be produced when RETURN A and RETURN B are logical 0 [+5V] and this occurs only when both print out devices have completed a character print out.

Decode/Encode Board.

Reference clock, Manual Entry & Decode/Encode Drive Logic Diagram 19727003.

When CALL A is at logical 0, removing the logical 1 clamp on the Bistable, and RUN A goes to logical 1, FF RUN sets such that Q is logical 1 and $\overline{Q}$ logical 0.

$\overline{Q}$ is fed via Link 1 [normally connected] to NAND gates $\overline{\&}4$ and $\overline{\&}5$ priming them. $\overline{\&}4$ output is routed to BCD to Decimal Board 1 and via $\overline{\&}5$ to BCD to Decimal Board 2. $\overline{Q}$ allows both 8 and $\overline{8}$ information to be fed to the BCD to Decimal, otherwise $\overline{Q}$ inhibits the decode of the serialised 4-bit highway.

$\overline{Q}$ also satisfies $\overline{\&}13$ [primed by CALL A], the logical 1 output setting the Monostable SSM1 to produce a PUNCH INSTRUCTION. The output unit now prints or punches out the information and produces a PUNCH READY pulse, the trailing edge of which,

via a pulse network, [I12 and $\overline{PA1}$] produces a logical 1 to clock over FF RUN giving Q logical 0 and $\overline{Q}$ logical 1. $\overline{Q}$ being logical 1 inhibits both $\overline{\&}4$ and $\overline{\&}5$ preventing operation of both BCD to Decimal boards until a further RUN A pulse sets FF RUN.

The next RUN A pulse will occur after a delay due to the Serialiser Logic, this delay allows print out to be inhibited after S11 has been reached. $\overline{S}12$ going to logical 1 inhibits $\overline{\&}15$ and $\overline{\&}16$ [D19727001] preventing further RUN pulses.

If a device which does not give a PUNCH READY pulse is used then the second Monostable, SSM2, allows this pulse to be simulated and depending on the device used a positive or negative pulse can be selected by connection of appropriate links.

Switching Facilities

SWA - 3 positions
OFF - Clamps ZERO line and Print Command A input to 0V; resets and holds all bistables on board 19729304 such that Q is logical 1, $\overline{Q}$ logical 0. No Print Commands can thus operate the Bistables.

1972 and 1978 - Releases 0V Clamp on both Print Command bistables and allows 1972 to accept both Print Commands.

1978 only - Clamps PRINT COMMAND 'A' input to 0V preventing Print Command A input, allows Print Command B to be accepted.

SWB - two positions [1978]
ON - Allows Print Command B to be accepted.

OFF - Clamps Print Command B input to 0V preventing Print Command B input and clamps CALL B line to 0V.

Power Supplies

Reference: Shift Register and Power Supply Circuit Diagram D19729106.

Mains transformer T1 has two 0-115V primary windings which may be connected in series or in parallel for 230V or 115V working, respectively, by means of MSP1.

The two secondary windings are full wave rectified to give a +5V regulated supply of 1A capability and a -10V stabilised supply, by Zener diode MR12, with a 60mA capability.

SECTION 4

TEST PROCEDURE

GENERAL

The following information details the testing of the LU1972 as a standard item producing a full read or punch out of all available characters. Links are detailed for all characters and for variations of code and patching reference should be made to Section 2.

TEST EQUIPMENT

The following test equipment is required:-

Oscilloscope

Facit 4070
Manual Entry Unit LU1960

TEST PROCEDURE

Ensure all links as detailed on the circuit diagrams are made.

Manual Entry

Connect output device and Manual Entry Unit. Ensure that link C-P6 is made on Board 'F'. Set SWA to centre position and SWB off. Enter characters set up on the 1960 unit.

Punch or Read out should be six characters as per 1960 edge switches. e.g. Set up 1, 2, 3, 4, 5, 6. When the entry button is depressed the punch out should be in this same order.

All decodes 0 to 15 can be checked by using these switches.

Note... When SWA is set to the OFF position zero state is conditioned.

Clock Data

Apply -10V through 1.5K to the clock data inputs as per PLB connections, clock inputs not used should be terminated at 0 to -1V.

Apply -ve edge 0V to -10V with a fall time of $\geq 2\mu S$
Provide Print Command A at PLB pin DD (-10V to 0V) with a risetime of $\geq 2\mu S$.
to PLB pin EE. (Clock Command)
Punch out should be 2 3 5 9 FC1 FC2
i.e. six characters where

Tens of hours	2
Units of hours	3
Tens of minutes	5
Units of minutes	9
FC1 C/R decode 10	FC1
FC2 LF decode 14	FC2

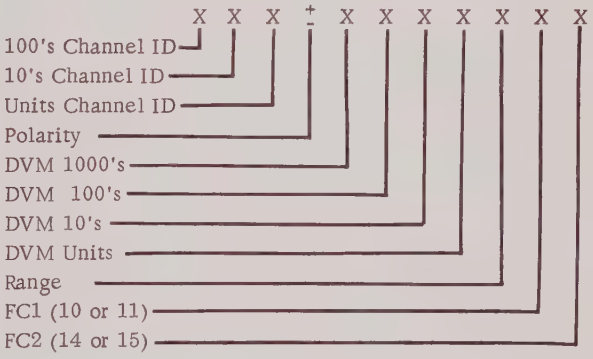
Main Data Word

The main data word is variable from a normal 11 character word to a 4 character word by patching links on Board F. The shift register always ends on S12, but the start point depends on the data start 'A' link position,

e.g.	Link A - P1	11 Character Word
	Link A - P4	8 Character Word
	Link A - P8	4 Character Word

Ensure that link A-P1 is in position and that the patching matrix is as shown on circuit diagram D19729306

Punch out should be



Fixed Character Coding

Terminate pins CC and FF (PLB) at 0V and apply a Print Command 'A' pulse.

The last two characters of the punch out should be:-

FC1 decode 11
FC2 decode 15

Apply -10V through 1.5K resistor to PLB pin CC and apply a Print Command 'A'. Punch out should be:-

FC1 decode 10
FC2 decode 15

Apply -10V through 1.5K to PLB pin FF and apply Print Command 'A'. Punch out should be:-

FC1 decode 10
FC2 decode 14

Auto Return

Set up the 1972 for a M.E., Clock, and Print Command 'A' and ensure that an Auto Return is generated at PLB pin t approximately 1mS after receiving the appropriate command.

Dual Serialiser Capability

The 1972 can accept two Print Commands at any one time from a CL2 system as a Routine and/or an Alarm Print Command. This dual capability is made use of when the 1972 is used with a 1978 unit. However, because of the closed loop sequence it is not possible to test fully the Print Command 'B' sequence.

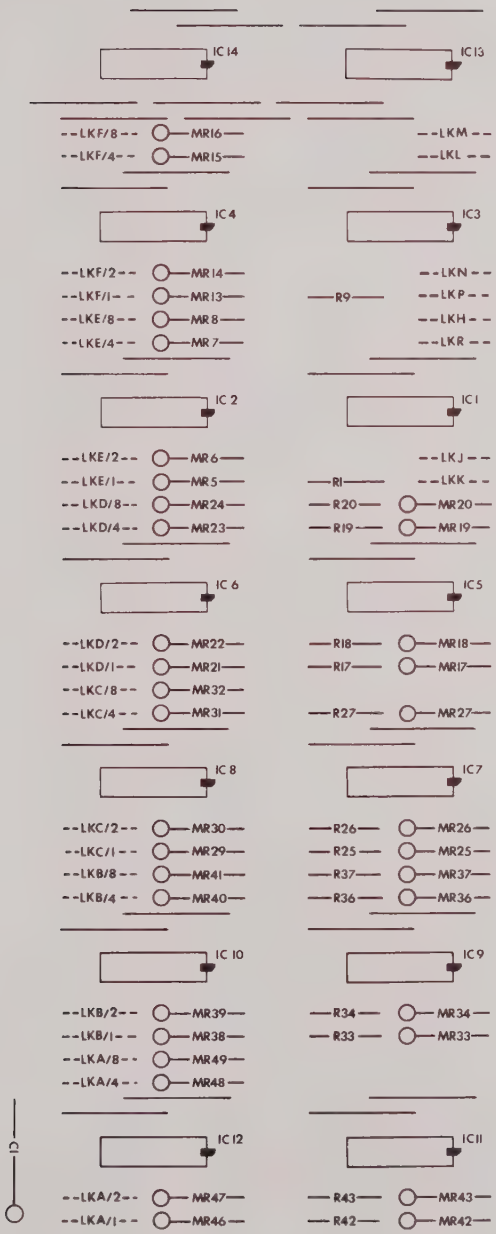
The following, will however test the "pick-up" and start point for the Print Command 'B' sequence.

Switch SWB to the ON position
Switch SWA to 1972 & 1978 position

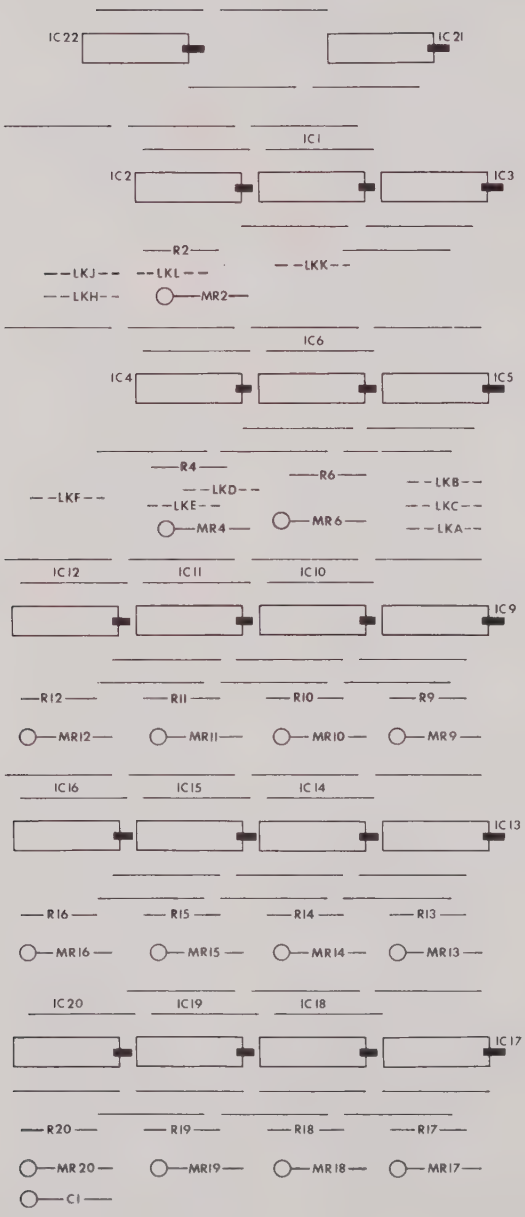
Apply a Print Command 'A' pulse, the Facit 4070 will punch all eleven characters and a Run B pulse will be obtained as soon as the 4th position of the Shift Register is reached i.e. Sx patched to S4.

SWA to the 1978 ONLY position.
Switch SWB to the ON position

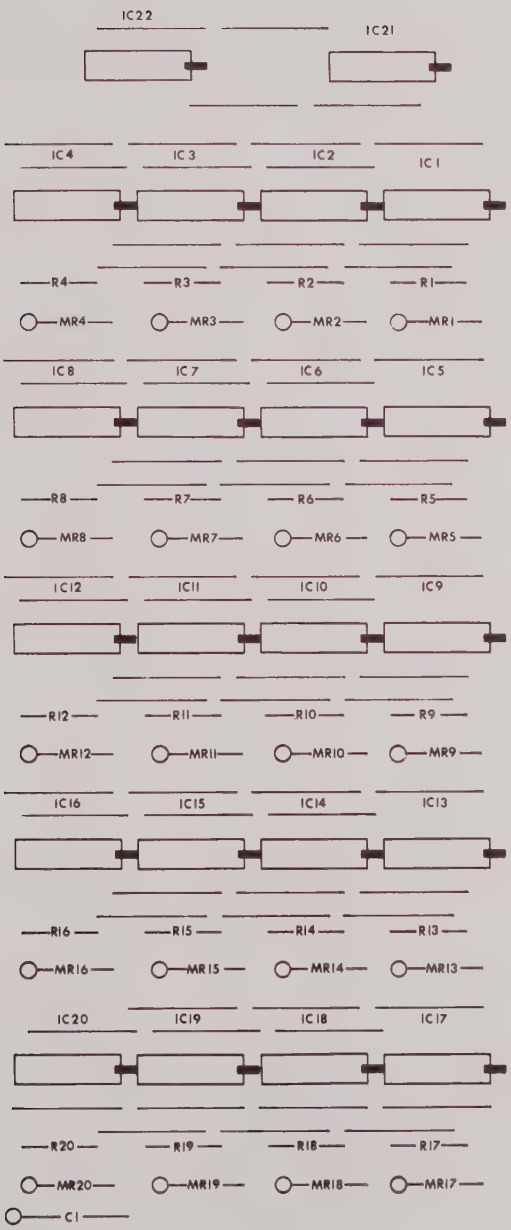
Apply a Print Command 'B' pulse to PLE pin D. Approximately 500 μS after the Print Command 'B' a Data Start 'B' pulse +5V to 0V will occur on pin 36, which will start the Shift Register on the S4 position, i.e. IC4 pin 6 goes to +5V and remains at +5V. The Shift Register will not step through its ring positions because no 'B' Driver Board is present. The 1972 will now have to be 'zeroed' (i.e. SWA to the OFF position) before the unit will accept another Print Command.



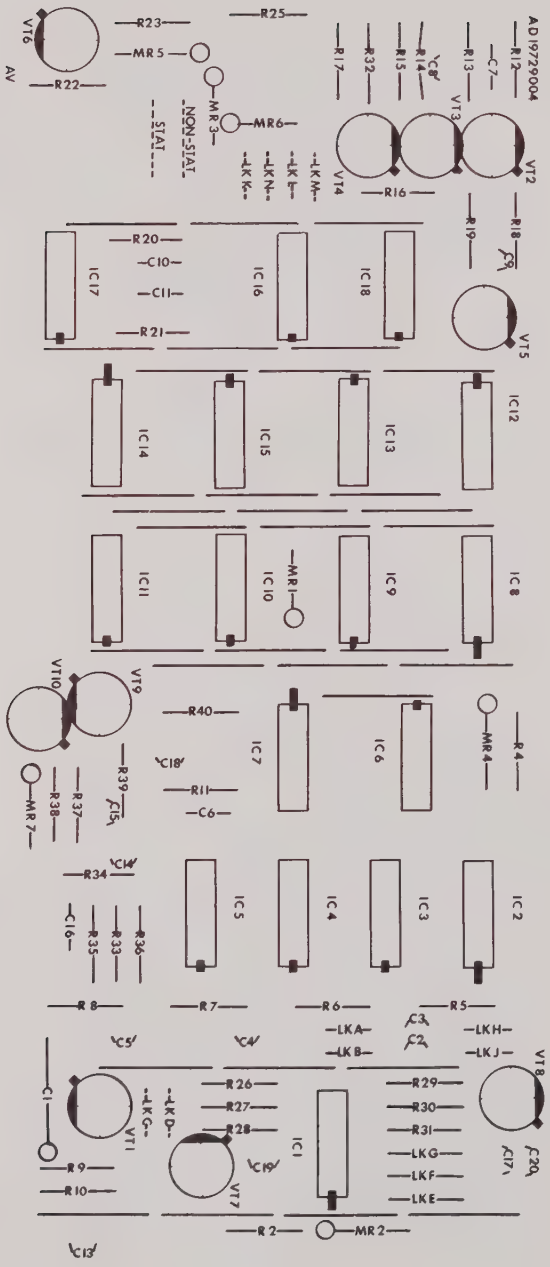
Component Location Printed Circuit Board 19729401



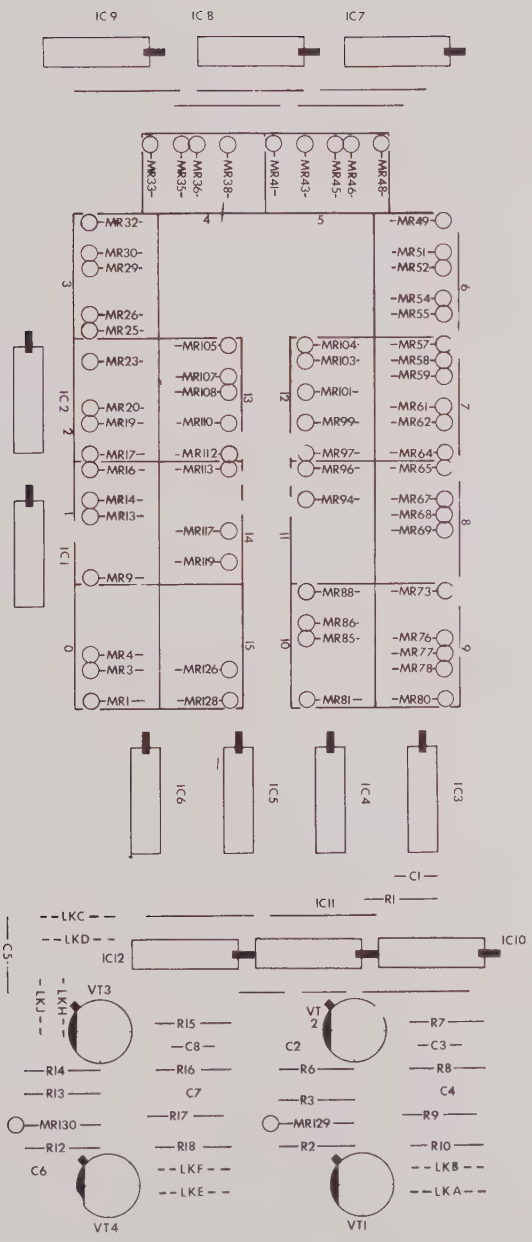
Component Location Printed Circuit Board 19729402



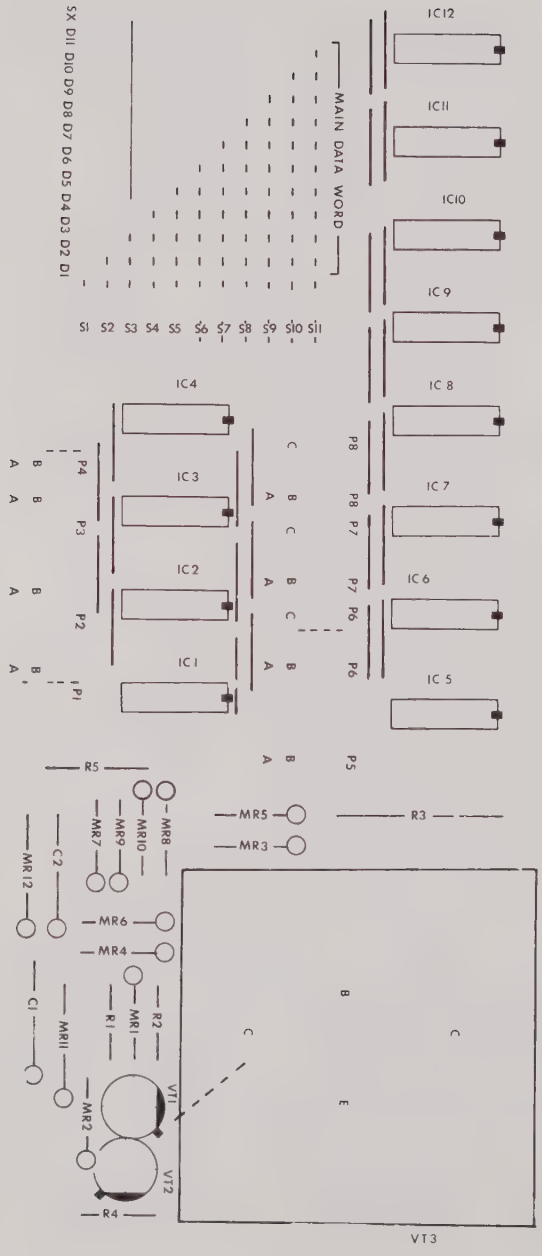
Component Location Printed Circuit Board 19729403



Component Location Printed Circuit Board 19729404



Component Location Printed Circuit Board 19729405



Component Location Printed Circuit Board 19729406

Component Parts List Abbreviations

Circuit References		Component Composition	
R	Fixed Resistor [Ω]	A	Capacitor Polystyrene Tubular
RNL	Non Linear Resistor [Ω]	B	Capacitor Polyester Tubular Metalised
RV	Variable Resistor [Ω]	C	Capacitor Polyester Tubular Foil
C	Capacitor [μF]	D	Capacitor Paper Foil
MR	Diode	E	Capacitor Paper Metalised
L	Inductor	F	Capacitor Ceramic Tubular
V	Valve	G	Capacitor Ceramic Disc
VT	Transistor	H	Capacitor Silver Mica
IC	Integrated Circuit	J	Capacitor Electrolytic Al.
RL	Relay	K	Capacitor Electrolytic Al. Plain Foil
S	Switch	L	Capacitor Electrolytic Tantalum
PL	Plug	M	Capacitor Variable Air Preset
SK	Socket	N	Capacitor Variable Ceramic Disc Preset
MSP	Mains Selector Panel	P	Capacitor Variable Tubular Preset
T	Transformer	R	Capacitor Variable Mica Compression Preset
FS	Fuse	S	Capacitor Polyester Special
ILP	Lamp	T	Capacitor Polycarbon
B	Battery	V	Resistor Metalised Film
M	Meter	W	Resistor Composition <5%
TP	Terminal Post	X	Resistor Composition >5%
LK	Link	Y	Resistor Wire Wound
X	Other Components	Z	Resistor Oxide Film >5%

Units and Values			
A	Amp	G	Giga [10^9]
F	Farad	M	Mega [10^6]
H	Henry	k	kilo [10^3]
Ω	Ohm	m	milli [10^{-3}]
V	Volts	μ	micro [10^{-6}]
W	Watts	p	pico [10^{-12}]

List of Printed Circuit Boards

Board Position	Description	Solartron Part No.
A	Clock/M.E. Data Board	19729001
B	Staticisor, Data 1, Board	19729002
C	Staticisor, Data 2, Board	19729003
D	Logic Board	19729004
E	Decode/Encode Drive Board	19729005
F	Shift Register and Power Supply Board.	19729006

Component Parts List for Chassis Assembly

Cct. Ref.	General Description				Solartron Part No.
C1	J	2500	25V	-20% +50%	208600189
C2	J	2500	25V	-20% +50%	208600189
PLA	Mains Plug				352303030
PLB	Conn. Shell Fixed 50 Way				354002330

Cct. Ref.	General Description	Solartron Part No.
PLC	Conn. Shell Fixed 34 Way	354002350
PLD	Conn. Shell Fixed 20 Way	354002380
PLE	Conn. Plug Fixed 7 Way	352307070
MSP1	Mains Selector Plug	399000060
FS1	Fuse 1 Amp	360203070
SWA	Switch D.P.D.T.	376000400
SWB	Switch S.P.S.T.	376000380
T1	Mains Transformer	B19720014

Component Parts List for Printed Circuit Board No. 19729001

Cct. Ref.	General Description				Solartron Part No.
R17	Z	6800	½W	5%	193536800
R18	Z	6800	½W	5%	193536800
R19	Z	6800	½W	5%	193536800
R20	Z	6800	½W	5%	193536800
R25	Z	6800	½W	5%	193536800
R26	Z	6800	½W	5%	193536800
R27	Z	6800	½W	5%	193536800
R33	Z	6800	½W	5%	193536800
R34	Z	6800	½W	5%	193536800
R36	Z	6800	½W	5%	193536800
R37	Z	6800	½W	5%	193536800
R42	Z	6800	½W	5%	193536800
R43	Z	6800	½W	5%	193536800
C1	L	.047	35V	10%	265944700
MR5 to MR8		SD3	Solartron		300522160
MR14 to MR27		SD3	Solartron		300522160
MR28 to MR34		SD3	Solartron		300522160
MR36 to MR43		SD3	Solartron		300522160
MR46 to MR49		SD3	Solartron		300522160
IC1 to IC14		SN15846N	Integrated Circuit		510000160

Component Parts List for Printed Circuit Board No. 19729002

Cct. Ref.	General Description				Solartron Part No.
R2	Z	6800	½W	5%	193536800
R4	Z	6800	½W	5%	193536800
R6	Z	6800	½W	5%	193536800
R9 to R20	Z	6800	½W	5%	193536800
C1	L	.047	35V	10%	265944700
MR2		SD3	Solartron		300522160
MR4		SD3	Solartron		300522160
MR6		SD3	Solartron		300522160
MR9 to MR20		SD3	Solartron		300522160
IC1 to IC6		SN15846N	Integrated Circuit		510000160
IC9 to IC22		SN15846N	Integrated Circuit		510000160

Component Parts List for Printed Circuit Board No. 19729003

Cct. Ref.	General Description				Solartron Part No.
R1 to R20	Z	6800	½W	5%	193536800
C1	L	.047	35V	10%	265944700
MR1 to MR20		SD3	Solartron		300522160
IC1 to IC22		SN15846N	Integrated Circuit		510000160

Component Parts List for Printed Circuit Board No. 19729004

Cct. Ref.	General Description				Solartron Part No.
R2	Z	6800	½W	5%	193536800
R4	Z	220	½W	5%	193522200
R5	Z	1000	½W	5%	193531000

Cct. Ref.	General Description				Solartron Part No.
R6	Z	1000	½W	5%	193531000
R7	Z	1000	½W	5%	193531000
R8	Z	1000	½W	5%	193531000
R9	Z	2200	½W	5%	193532200
R10	Z	10K	½W	5%	193541000
R11	Z	220	½W	5%	193522200
R12	Z	10K	½W	5%	193541000
R13	Z	2200	½W	5%	193532200
R14	Z	10K	½W	5%	193541000
R15	Z	2200	½W	5%	193532200
R16	Z	10K	½W	5%	193541000
R17	Z	2200	½W	5%	193532200
R18	Z	10K	½W	5%	193541000
R19	Z	2200	½W	5%	193532200
R20	Z	220	½W	5%	193522200
R21	Z	220	½W	5%	193522200
R22	Z	3300	½W	5%	193533300
R23	Z	270	½W	5%	193522700
R25	Z	470	½W	5%	193524700
R26	Z	22K	½W	5%	193542200
R27	Z	56K	½W	5%	193545600
R28	Z	4700	½W	5%	193534700
R29	Z	22K	½W	5%	193542200
R30	Z	56K	½W	5%	193545600
R31	Z	4700	½W	5%	193534700
R32	Z	2200	½W	5%	193532200
R33	Z	1000	½W	5%	193531000
R34	Z	6800	½W	5%	193536800
R35	Z	12K	½W	5%	193541200
R36	Z	1000	½W	5%	193531000
R37	Z	10K	½W	5%	193541000
R38	Z	39K	½W	5%	193543900
R39	Z	39K	½W	5%	193543900
R40	Z	10M	½W	10%	172371000
C1	L	.047	35V	10%	265944700
C2	G	1000p	500V	-20% +80%	241031000
C3	G	1000p	500V	-20% +80%	241031000
C4	G	1000p	500V	-20% +80%	241031000
C5	G	1000p	500V	-20% +80%	241031000
C6	G	0.1	10V	+100% -0%	241751000
C7	G	0.1	10V	+100% -0%	241751000
C8	G	3300p	500V	-20% +80%	241033300
C9	G	.01	18V	-25% +50%	241841000
C10	G	0.1	10V	+100% -0%	241751000
C11	G	0.1	10V	+100% -0%	241751000
C13	G	.01	18V	-25% +50%	241841000
C14	G	560p	500V	10%	208450075
C15	G	560p	500V	10%	208450075
C16	B	0.22	63V	10%	225152200
C17	G	1000p	500V	-20% +80%	241031000
C18	G	.01	18V	-25% +50%	241841000
C19	G	1000p	500V	-20% +80%	241031000
C20	G	1000p	500V	-20% +80%	241031000
MR1 to MR4		SD3	Solartron		300522160
MR5		SZD12	Solartron		300521480
MR6		SD3	Solartron		300522160
MR7		SD3	Solartron		300522160
VT1 to VT10		BC107/S	Transistor		300553320
IC1	936		Integrated Circuit		510000290
IC2 to IC5	SN15845N		Integrated Circuit		510000150
IC6	962		Integrated Circuit		510000200
IC7	936		Integrated Circuit		510000290
IC8 to IC11	SN15845N		Integrated Circuit		510000150
IC12	SN15846N		Integrated Circuit		510000160
IC13			Integrated Circuit		510000290
IC14	SN15846N		Integrated Circuit		510000160
IC15	SN15846N		Integrated Circuit		510000160
IC16	SN15846N		Integrated Circuit		510000160
IC17	936		Integrated Circuit		510000290
IC18	936		Integrated Circuit		510000290

Component Parts List for Printed Circuit Board No. 19729005

Cct. Ref.	General Description				Solartron Part No.
R1	Z	220	½W	5%	193522200
R2	Z	10K	½W	5%	193531000
R3	Z	39K	½W	5%	193543900
R6	Z	39K	½W	5%	193543900
R7	Z	1000	½W	5%	193531000
R8	Z	12K	½W	5%	193541200
R9	Z	6800	½W	5%	193536800
R10	Z	1000	½W	5%	193531000
R12	Z	10K	½W	5%	193541000
R13	Z	39K	½W	5%	193543900
R14	Z	39K	½W	5%	193543900
R15	Z	1000	½W	5%	193531000
R16	Z	12K	½W	5%	193541200

R17	Z	6800	½W	5%	193536800
R18	Z	1000	½W	5%	193531000
C1	B	0.15	63V	10%	225151500
C2	G	560p	500V	10%	208450075
C3	B	0.22	63V	10%	225152200
C4	G	560p	500V	10%	208450075
C5	L	.047	35V	10%	265944700
C6	G	560p	500V	10%	208450075
C7	G	560p	500V	10%	208450075
C8	B	0.22	63V	10%	225152200

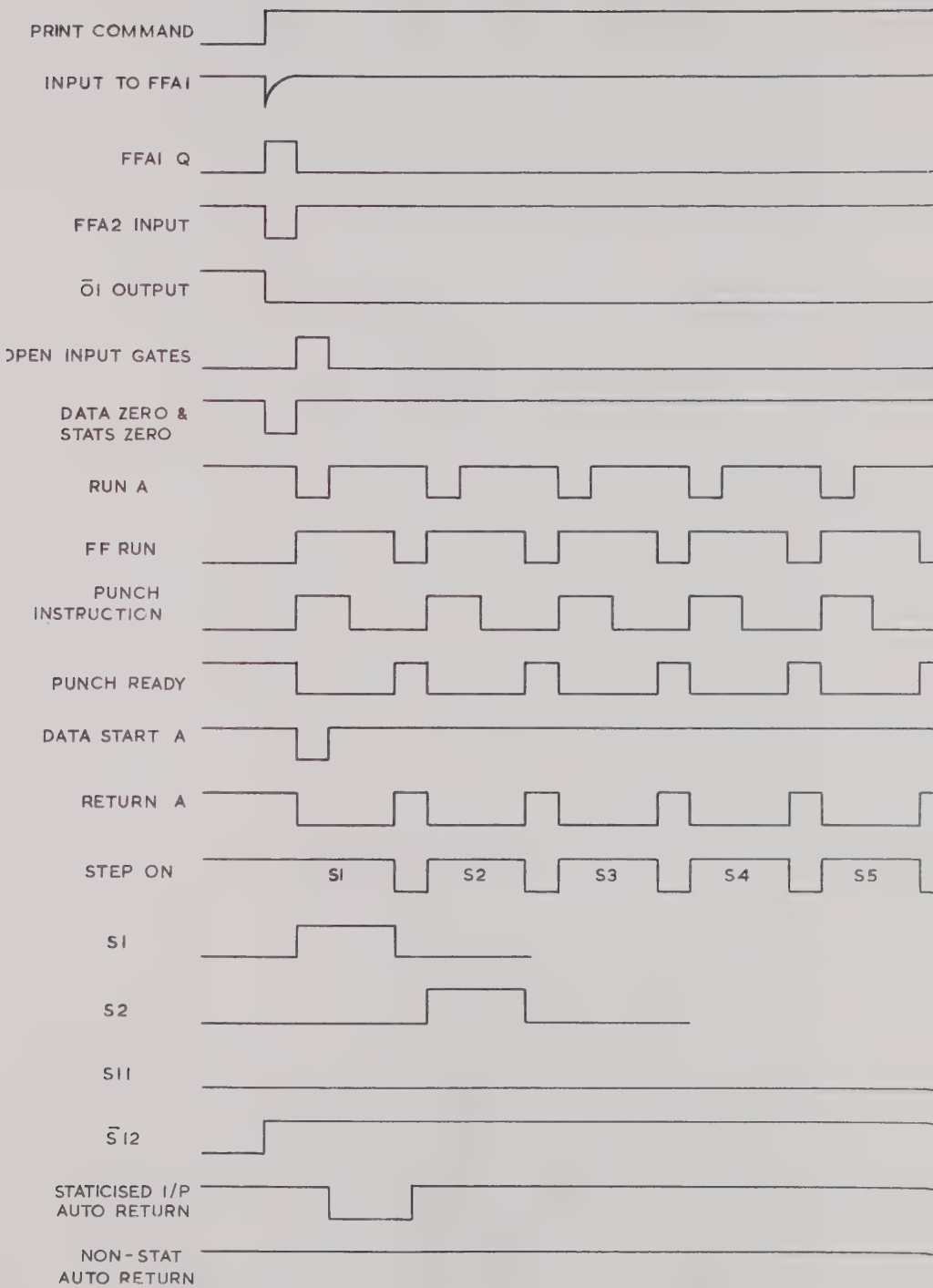
All diodes fitted are:

	SD3	Solartron	300522160
VT1 to VT4	BC107/S	Mullard	300553320
IC1	SN15846N	Integrated Circuit	510000160
IC2	SN15846N	Integrated Circuit	510000160
IC3 to IC6	SN15832N	Integrated Circuit	510000120
IC7	9301	Integrated Circuit	510000260
IC8	9301	Integrated Circuit	510000260
IC9	SN15846N	Integrated Circuit	510000160
IC10	SN15846N	Integrated Circuit	510000160
IC11	SN15845N	Integrated Circuit	510000150
IC12	SN15832N	Integrated Circuit	510000120

Component Parts List for Printed Circuit Board No. 19729006

Cct. Ref.	General Description				Solartron Part No.
R1	Z	2200	½W	5%	193532200
R2	Z	150	½W	5%	193521500
R3	Y	4.3	6W	5%	173704300
R4	Z	4700	½W	5%	193534700
R5	Y	82	2.5W	5%	173418200
C1	L	.047	35V	10%	265944700
C2	L	.047	35V	10%	265944700
MR1	SZD 2.7		Solartron		300523870
MR2	SZD 6.2		Solartron		300521240
MR3 to MR10	IN4002		Motorola		300522510
MR11	Z2A56F		STC		300524390
MR12	Z2A100F		STC		300522120

Cct. Ref.	General Description		Solartron Part No.
VT1	SM6526	Transistor	300552990
VT2	BC107/S	Mullard	300553320
VT3	2N3055	Transistor	300552340
IC1 to IC12	SN15845N	Integrated Circuit	510000150


PRINT COMMAND
INPUT TO FFA1
FFA1 Q
FFA2 INPUT
$\bar{O}$1 OUTPUT
OPEN INPUT GATES
DATA ZERO & STATS ZERO
RUN A
FF RUN
PUNCH INSTRUCTION
PUNCH READY
DATA START A
RETURN A
STEP ON
S1
S2
S3
S4
S5
S1
S2
S11
$\bar{S}$12
STATICISED I/P AUTO RETURN
NON-STAT AUTO RETURN

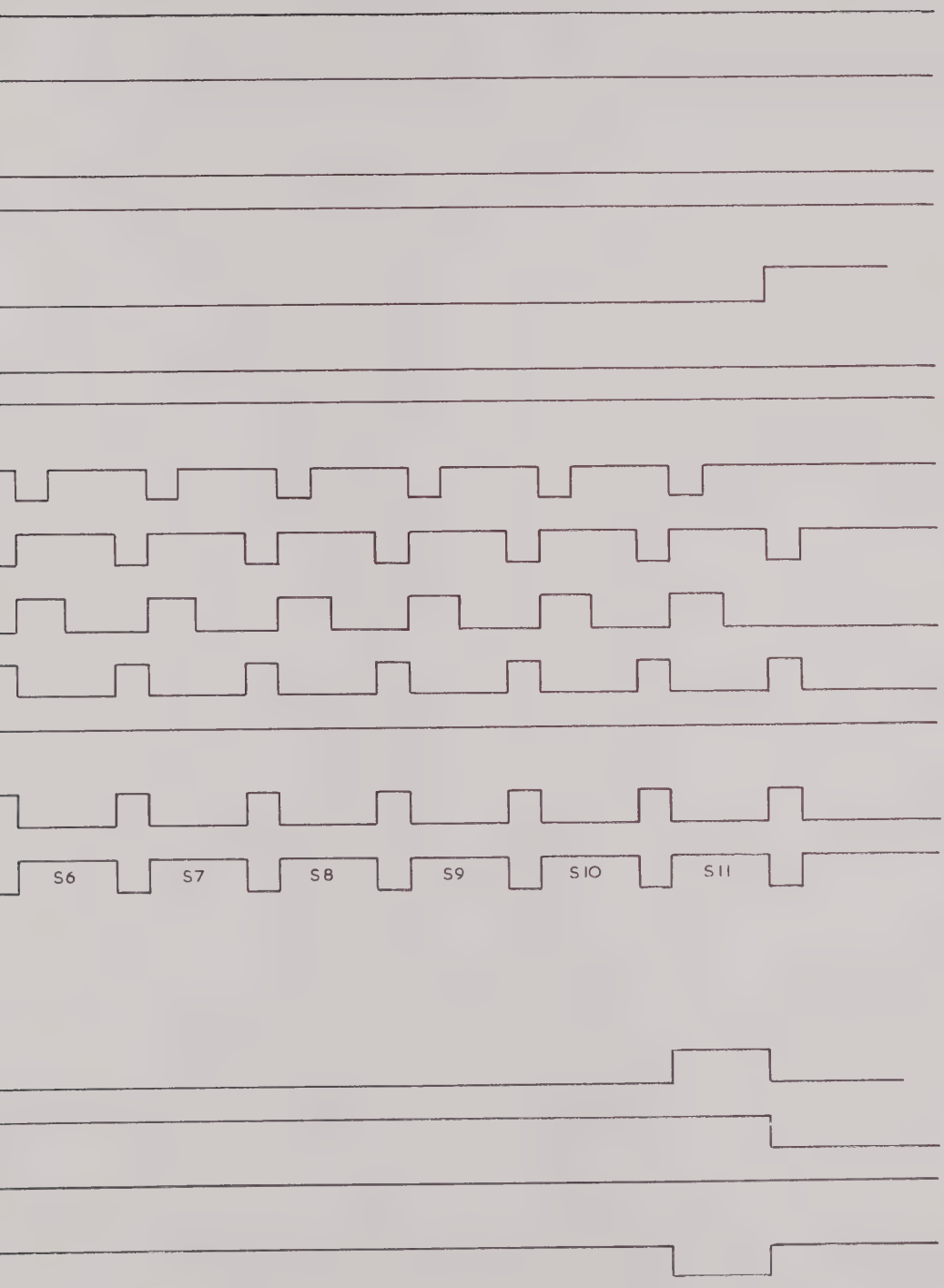
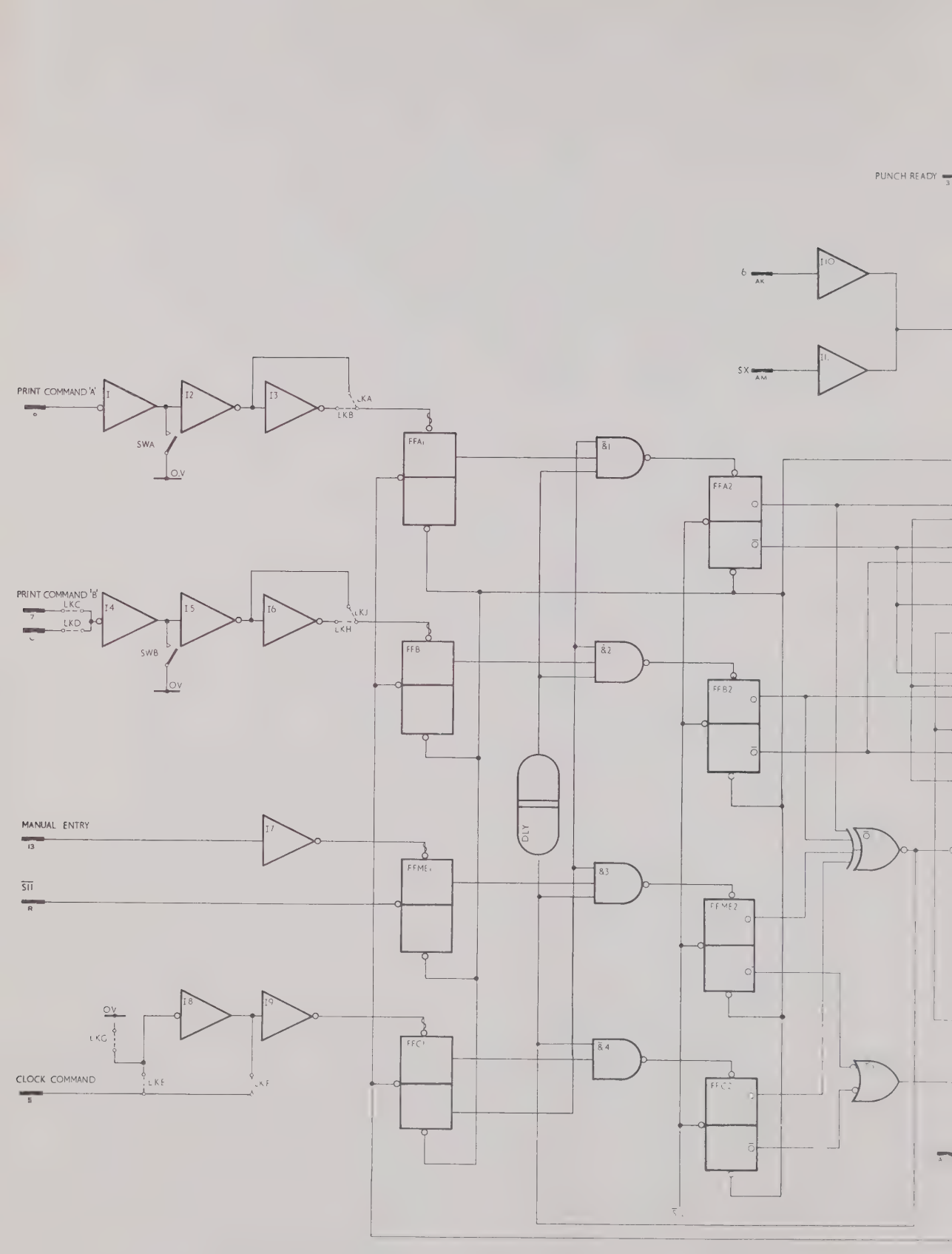


Figure 4.1 Timing Diagram


PUNCH READY
PRINT COMMAND 'A'
PRINT COMMAND 'B'
MANUAL ENTRY
CLOCK COMMAND
SWA
SWB
LKA
LKB
LKC
LKD
LKE
LKF
LKG
LKH
LKJ
I
I2
I3
I4
I5
I6
I7
I8
I9
I10
I11
FFA1
FFA2
FFB1
FFB2
FFME1
FFME2
FFC1
FFC2
&1
&2
&3
&4
DLY

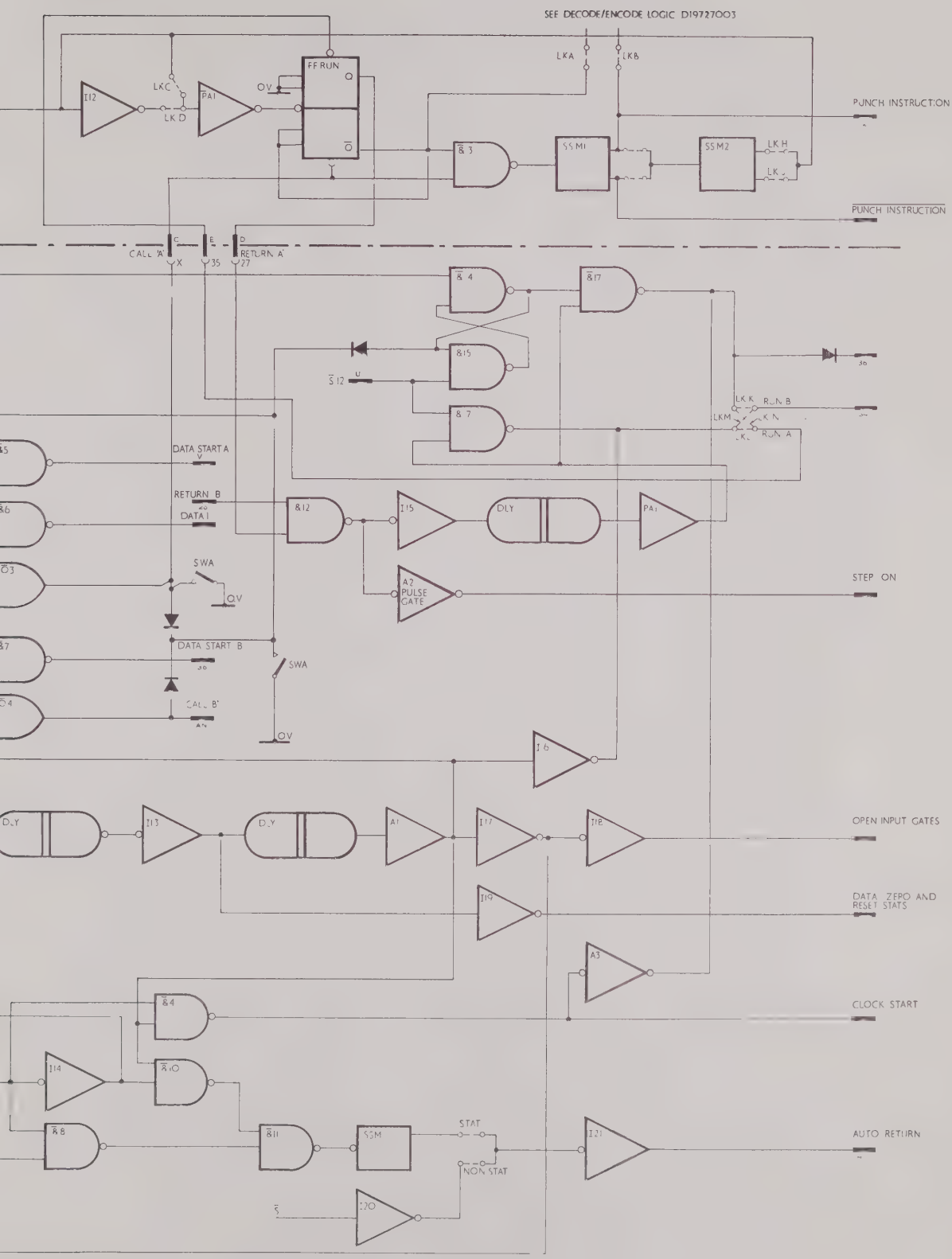
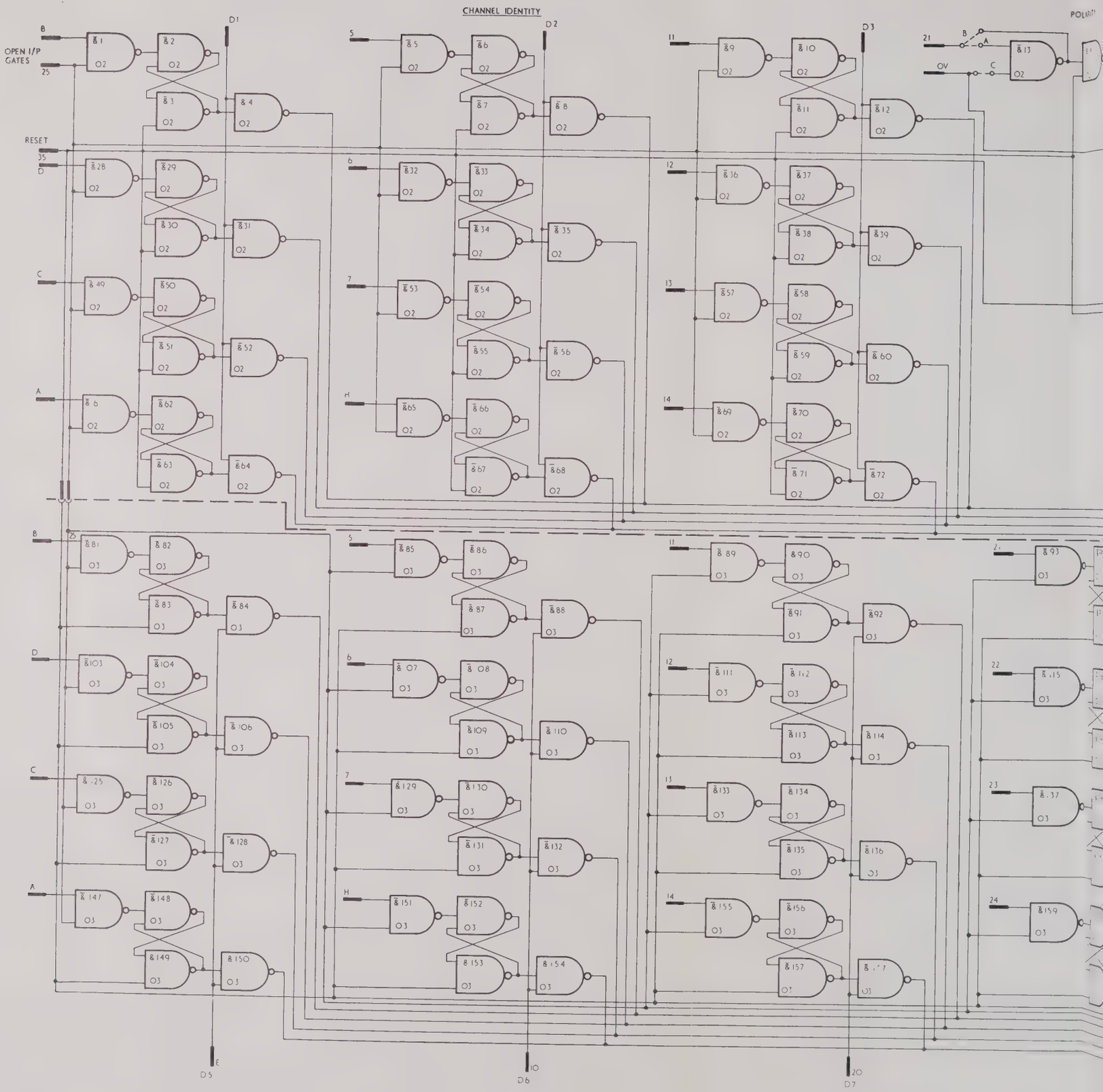


Figure 4.2 Serialiser Control Logic Diagram D 19727001


CHANNEL IDENTITY
OPEN I/P GATES
RESET
DVM READING

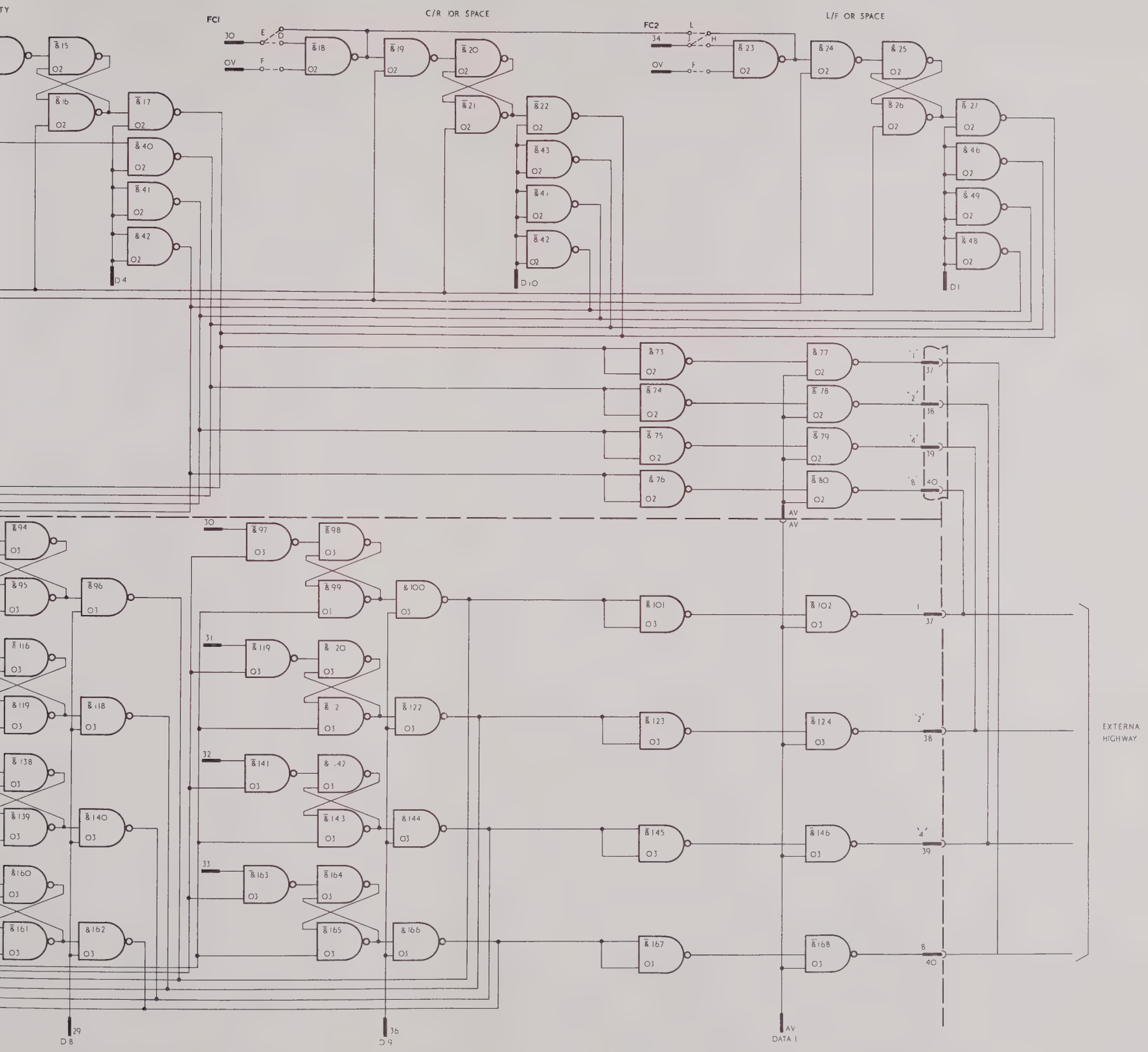
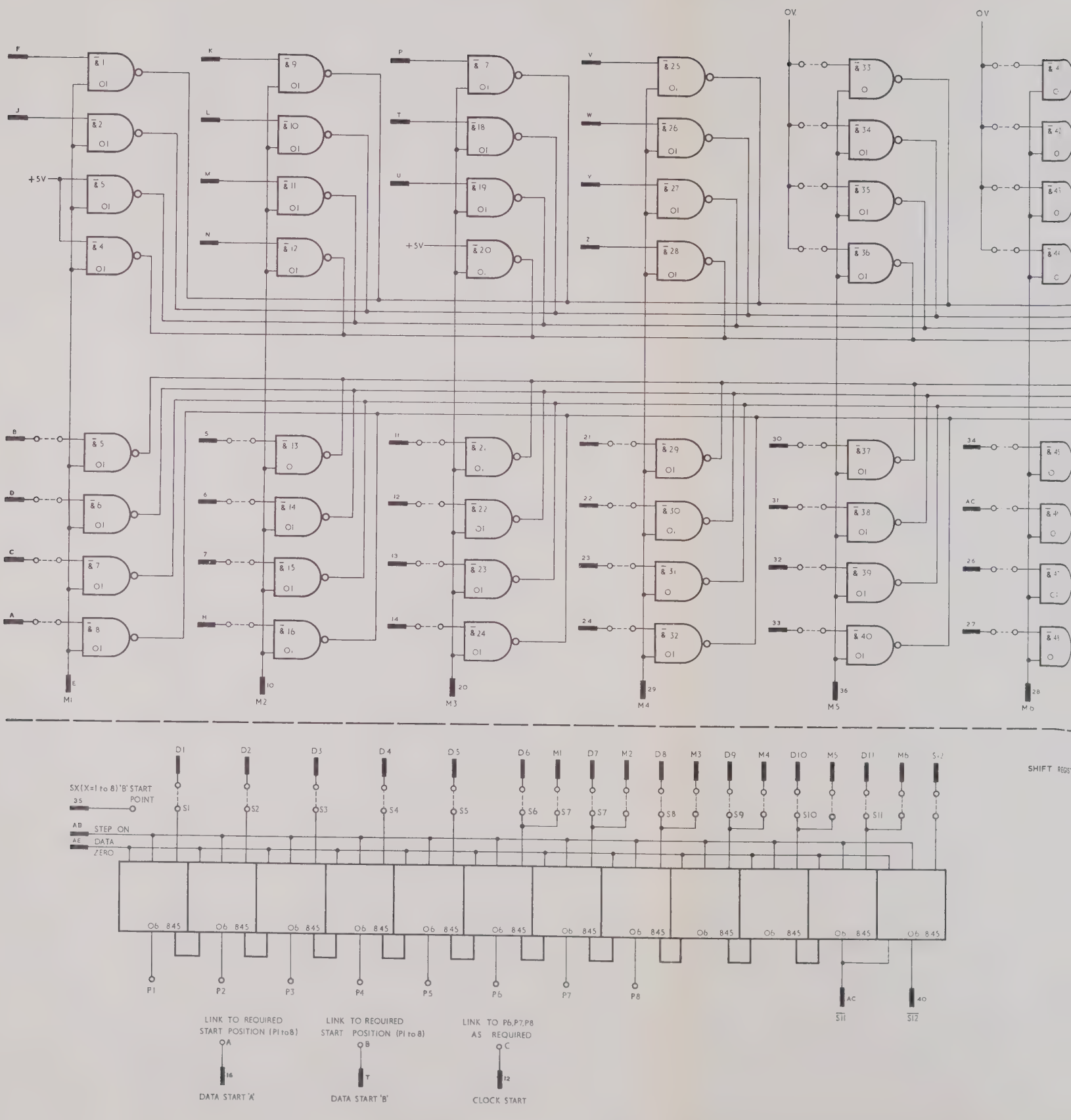


Figure 4.3 Staticisor Logic Diagram E 19727002


+5V
0V
M1
M2
M3
M4
M5
M6
SX(X=1 to 8)'B' START POINT
STEP ON
DATA ZERO
LINK TO REQUIRED START POSITION (P1 to 8)
DATA START 'A'
LINK TO REQUIRED START POSITION (P1 to 8)
DATA START 'B'
LINK TO P6,P7,P8 AS REQUIRED
CLOCK START
SHIFT REGIS

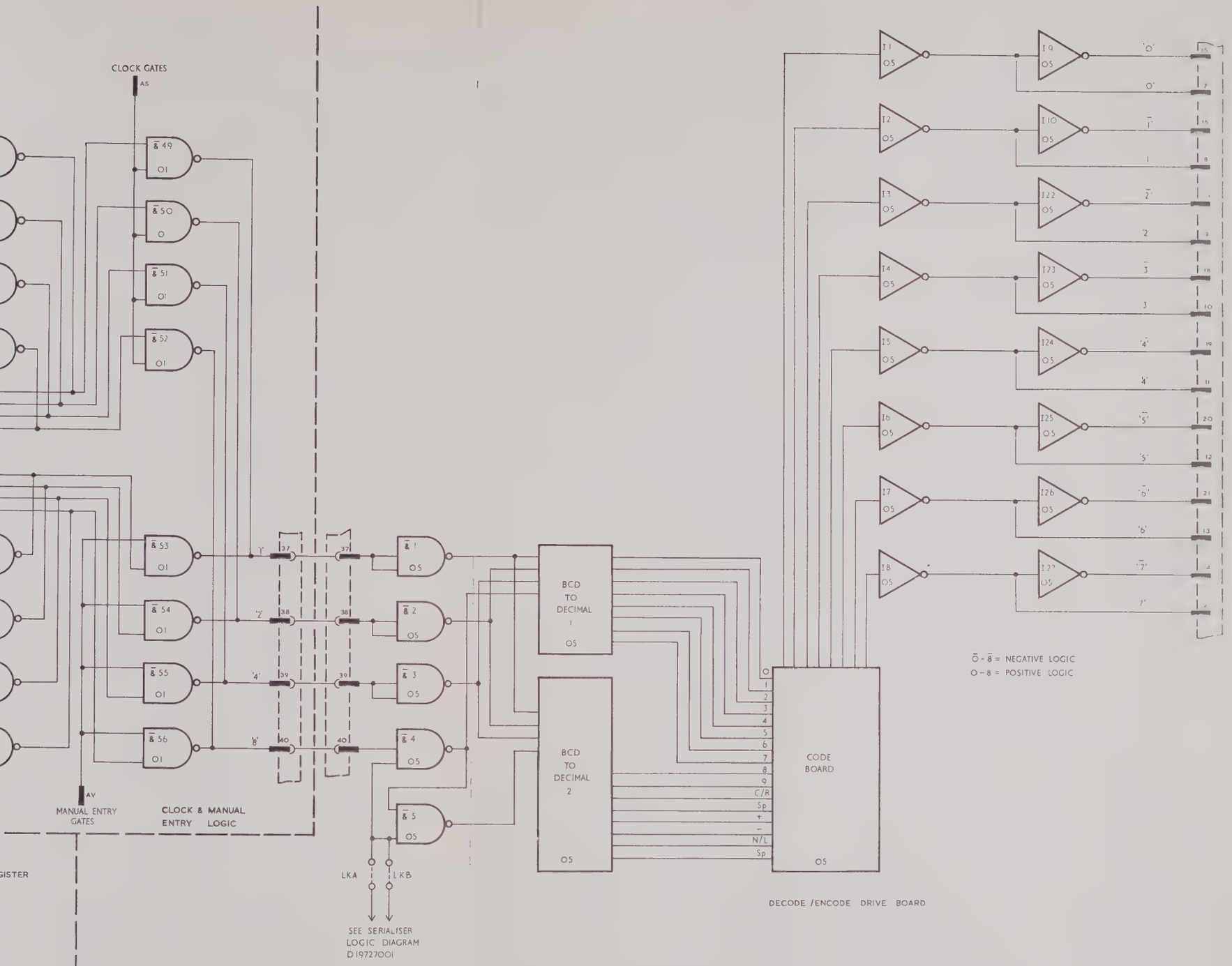
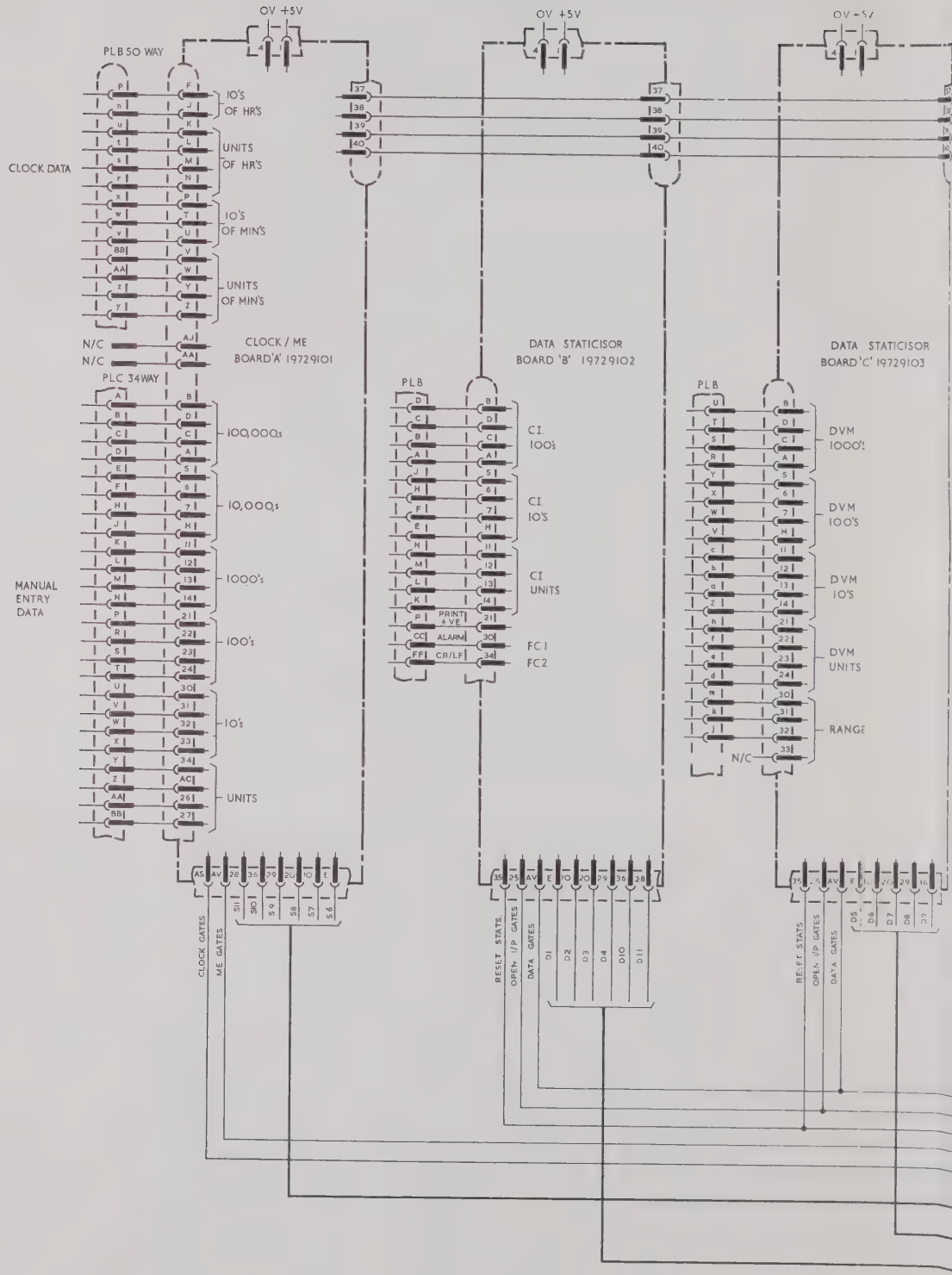
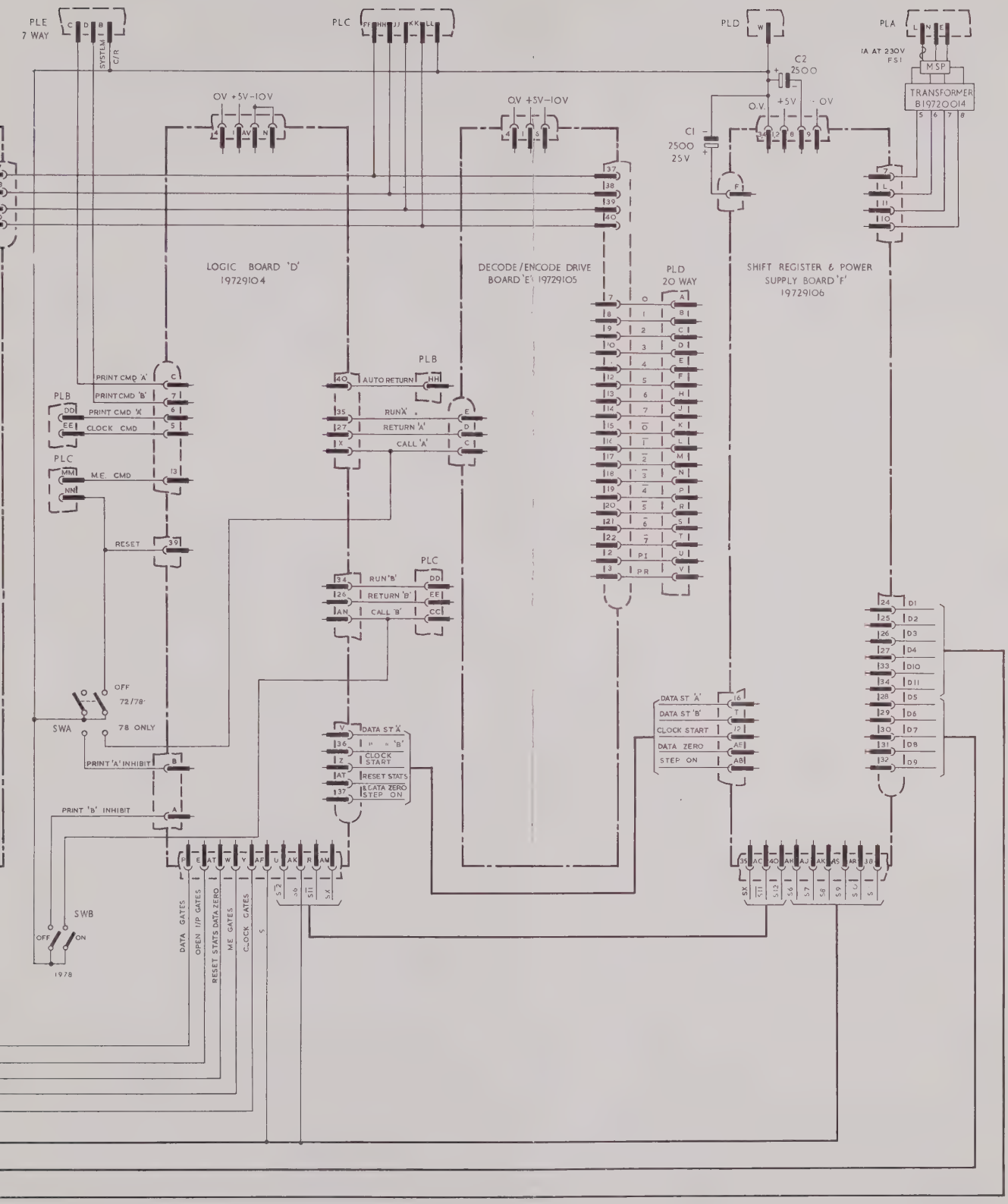


Figure 4.4 Clock, M/E and Decode/Encode Logic Diagram E19727003

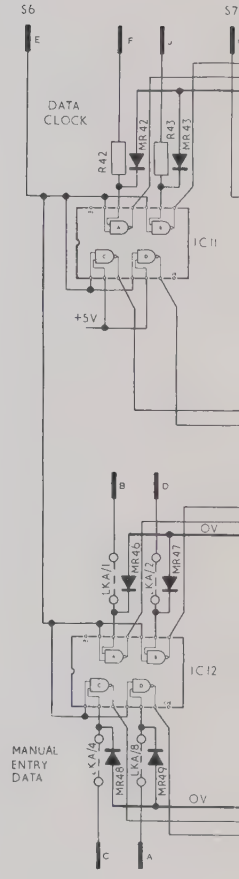

OV +5V
OV +5V
OV +5V
PLB 50 WAY
CLOCK DATA
10'S OF HR'S
UNITS OF HR'S
10'S OF MIN'S
UNITS OF MIN'S
N/C
N/C
CLOCK / ME BOARD 'A' 19729101
PLC 34WAY
MANUAL ENTRY DATA
100,000's
10,000's
1000's
100's
10's
UNITS
DATA STATICISOR BOARD 'B' 19729102
PLB
CI 100's
CI 10'S
CI UNITS
PRINT +VE
ALARM
CR/LF
FC1
FC2
DATA STATICISOR BOARD 'C' 19729103
PLB
DVM 1000's
DVM 100'S
DVM 10'S
DVM UNITS
RANGE
N/C
CLOCK GATES
ME GATES
RESET STATS.
OPEN I/P GATES
DATA GATES
D1
D2
D3
D4
D10
D11
RESET STATS.
OPEN I/P GATES
DATA GATES
D5
D6
D7
D8
D9



28 7 69

Figure 4.5 Interconnection Diagram

D19727005



NOTES :–

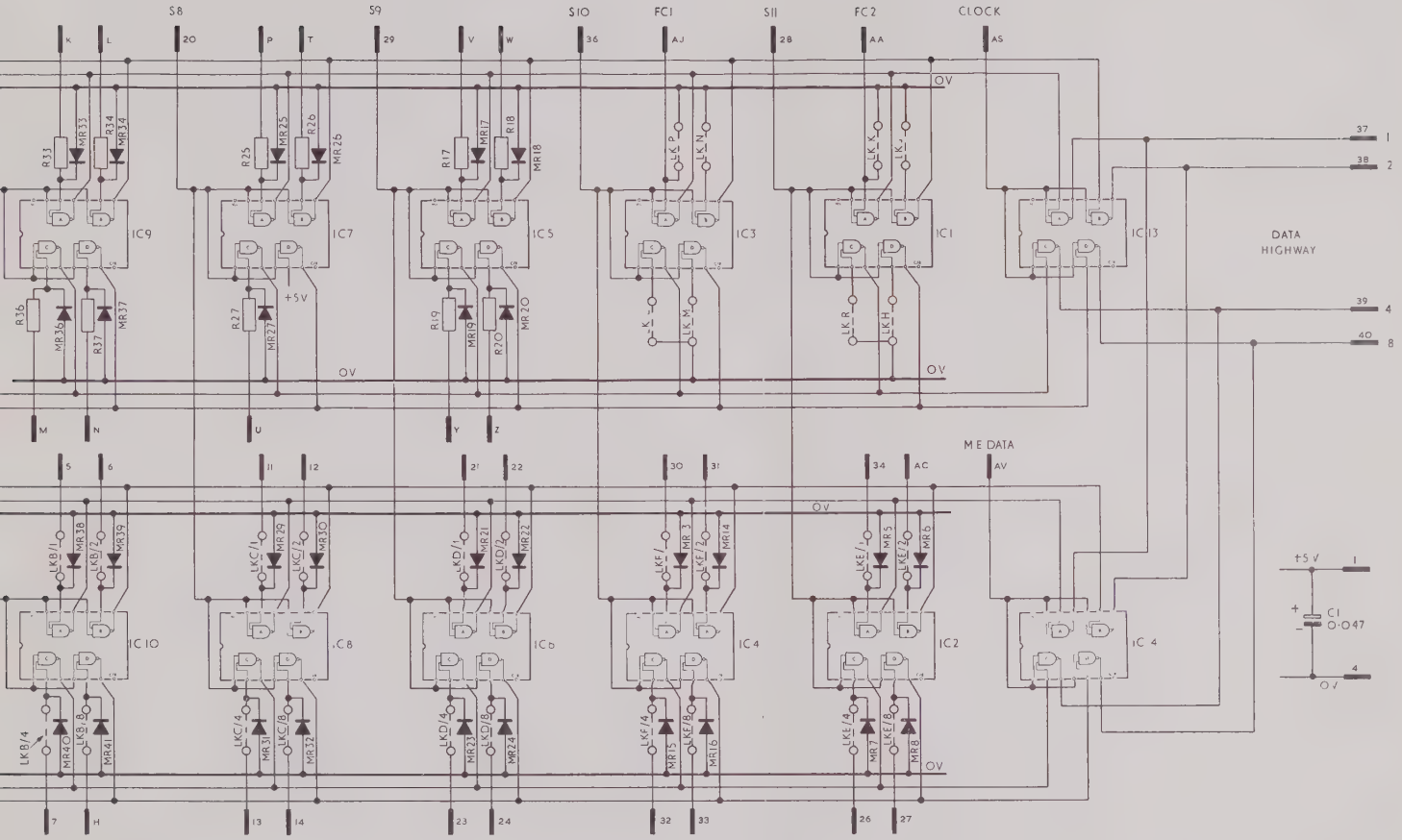
1 ALL RESISTORS 6·8K

2 ALL DIODES SD3

3 M E INPUTS HAVE LINKS F

4 ON CLOCK DATA N/C ON
TO DECODE CR AS FC1, UN
LF AS FC2 LINKS JR 6 H J

5. CLOCK DATA 2359 FC1, F



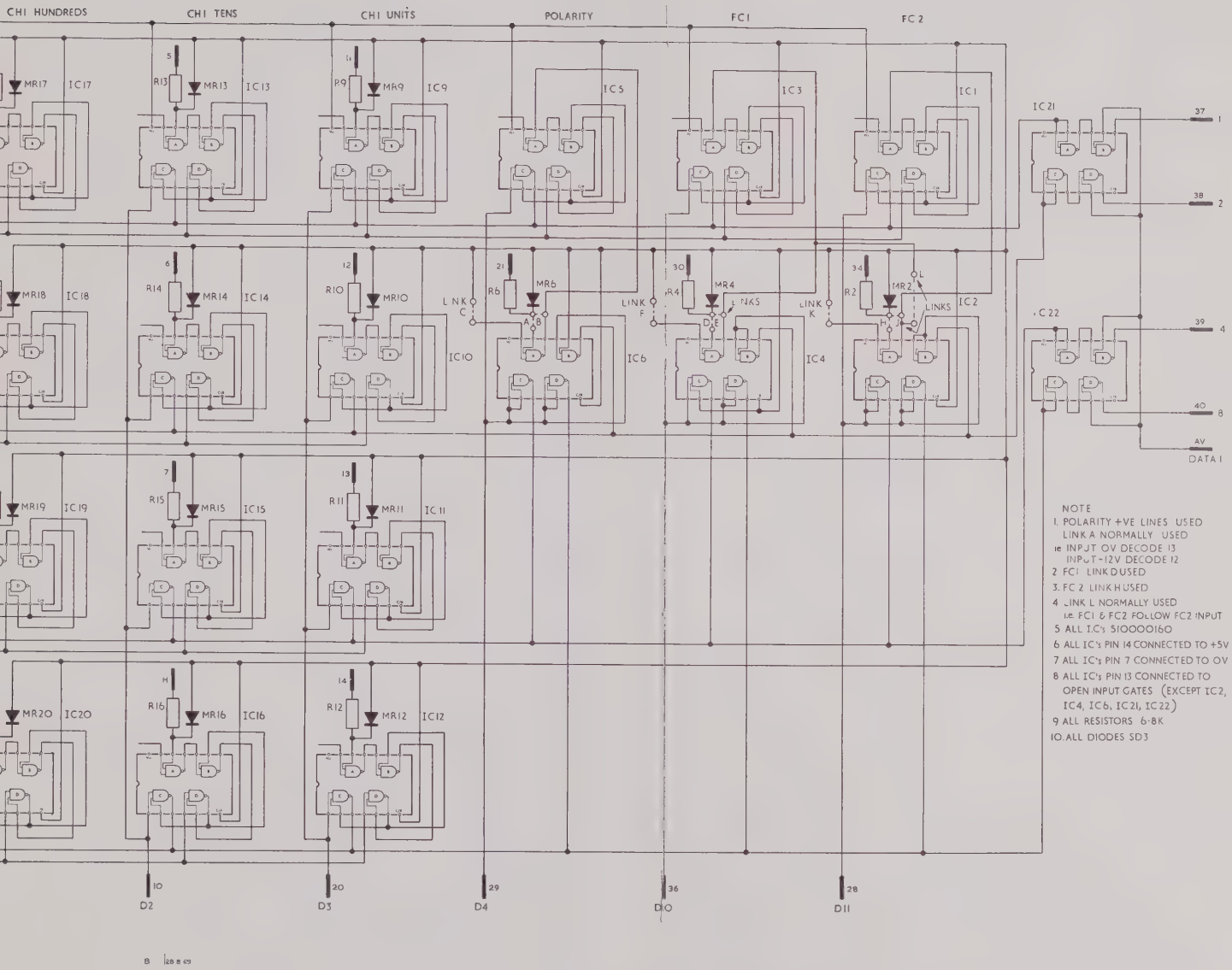
6 MANUAL ENTRY 999999
7 ALL I.Cs SN15846N
8 IC PIN 14 +5V ALL I.C's
IC PIN 7 0V ALL I.C's

R O TO +5V LEVEL INPUTS
INS AJ, AA IN NORMAL SYSTEM,
S MN USED
ED
2

B 30-6-69

Figure 4.6 Clock and M/E Circuit Diagram C 19729301

+5V
1
4
0V
25
OPEN INPUT GATES
RESET STAT
35
+5V
C1
·047
0V

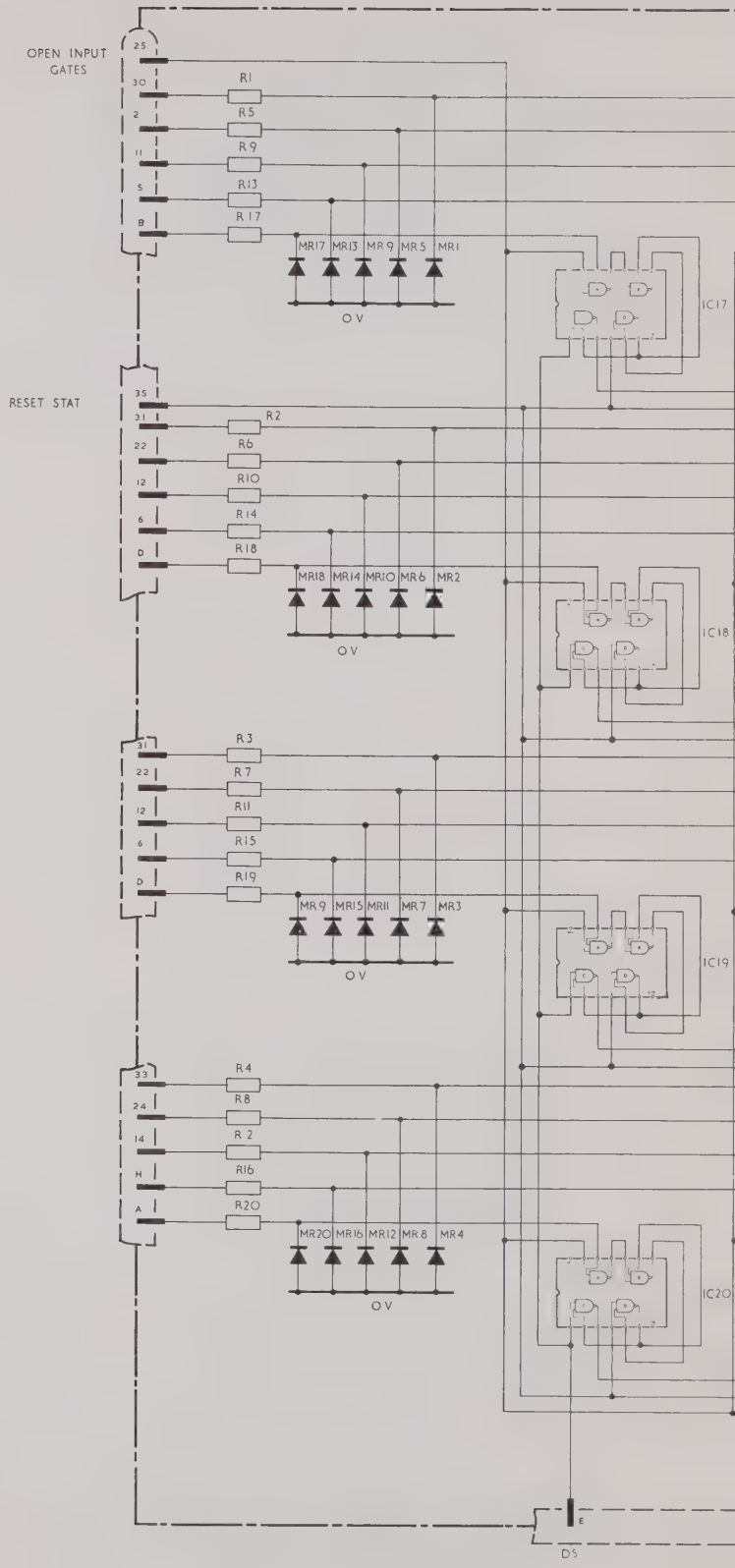


NOTE

1. POLARITY +VE LINES USED
   LINK A NORMALLY USED
   ie INPUT 0V DECODE 13
   INPUT -12V DECODE 12
2. FC1 LINK D USED
3. FC 2 LINK H USED
4. LINK L NORMALLY USED
   i.e. FC1 & FC2 FOLLOW FC2 INPUT
5. ALL I.C's 51000016O
6. ALL IC's PIN 14 CONNECTED TO +5V
7. ALL IC's PIN 7 CONNECTED TO 0V
8. ALL IC's PIN 13 CONNECTED TO OPEN INPUT GATES (EXCEPT IC2, IC4, IC6, IC21, IC22)
9. ALL RESISTORS 6·8K
10. ALL DIODES SD3

B 28 8 69

Figure 4.7 Staticisor Board 1 Circuit Diagram C 19729302


OPEN INPUT GATES
RESET STAT
25
30
2
11
5
8
35
31
22
12
6
D
31
22
12
6
D
33
24
14
H
A
R1
R5
R9
R13
R17
R2
R6
R10
R14
R18
R3
R7
R11
R15
R19
R4
R8
R12
R16
R20
MR17 MR13 MR9 MR5 MR1
MR18 MR14 MR10 MR6 MR2
MR9 MR15 MR11 MR7 MR3
MR20 MR16 MR12 MR8 MR4
0 V
IC17
IC18
IC19
IC20
E
DS

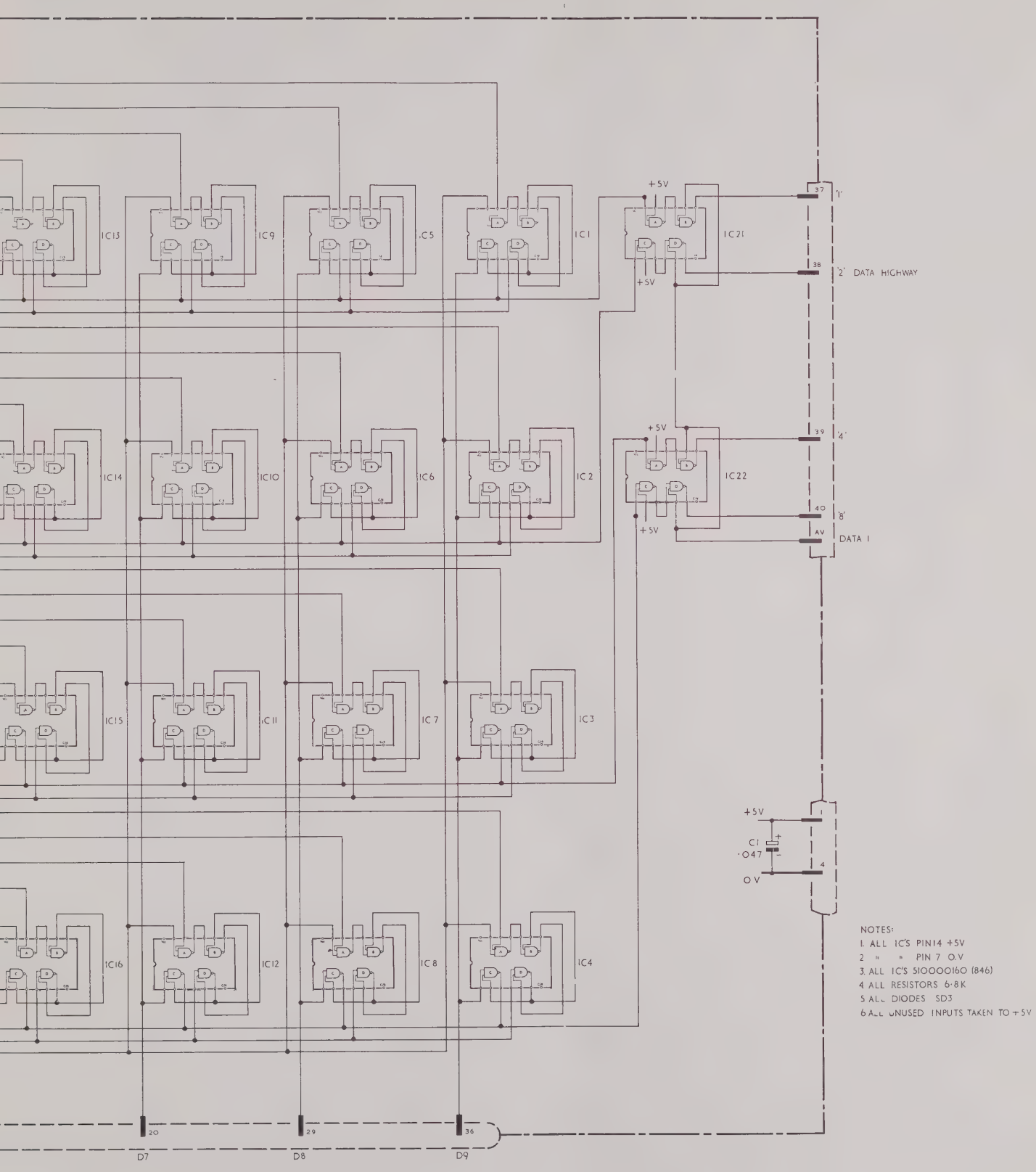
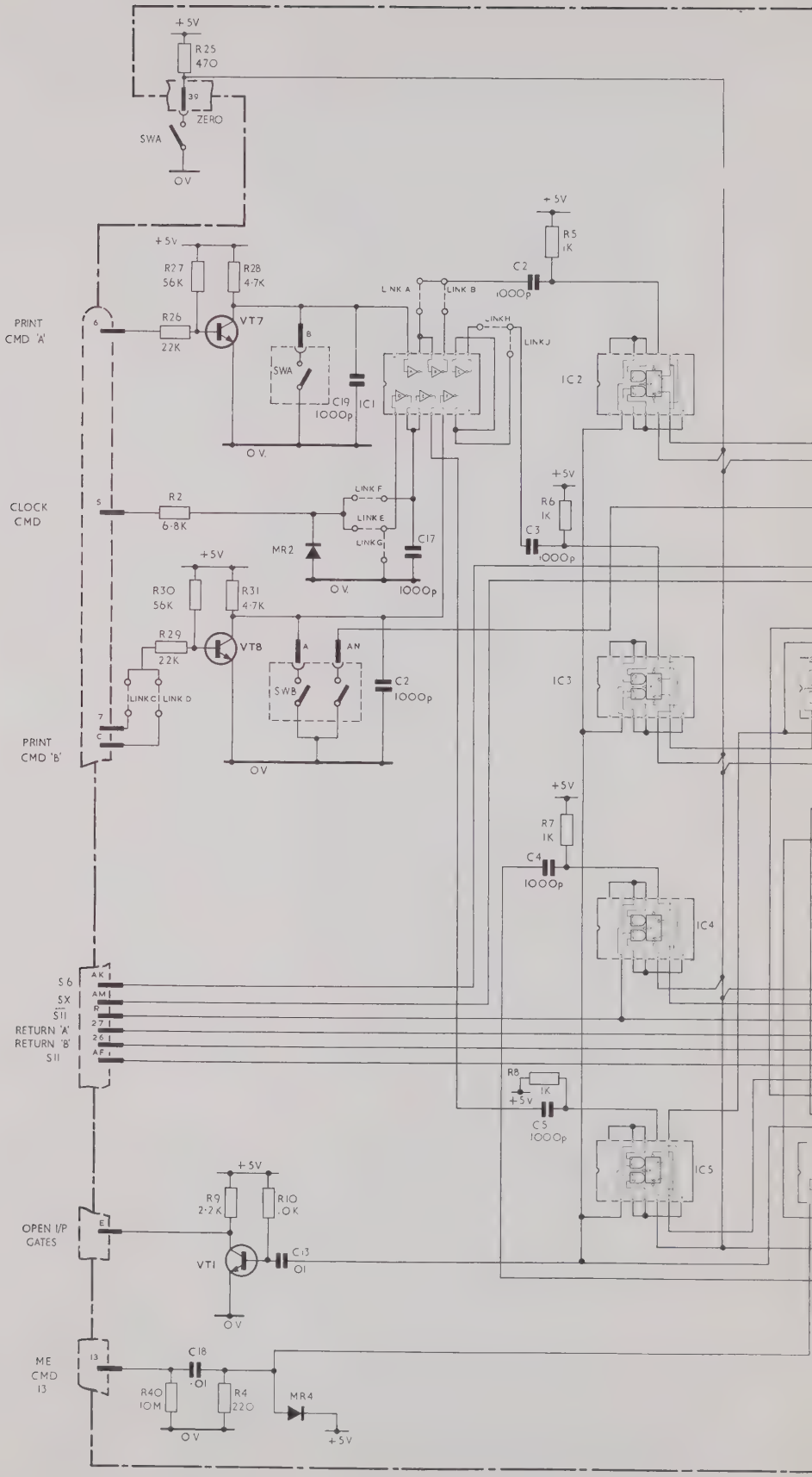


Figure 4.8 Staticisor Board 2 Circuit Diagram

D19729303


+5V
R25
470
39
ZERO
SWA
0V
+5V
R27
56K
R28
4·7K
R26
22K
VT7
PRINT
CMD 'A'
6
B
SWA
C19
1000p
IC1
0V.
+5V
R5
1K
C2
1000p
LINK A
LINK B
LINK H
LINK J
IC2
CLOCK
CMD
5
R2
6·8K
LINK F
LINK E
LINK G
MR2
C17
0V.
1000p
+5V
R6
1K
C3
1000p
+5V
R30
56K
R31
4·7K
R29
22K
VT8
A
AN
SWB
C2
1000p
LINK C
LINK D
7
C
PRINT
CMD 'B'
0V
IC3
+5V
R7
1K
C4
1000p
IC4
S6
SX
S11
RETURN 'A'
RETURN 'B'
S11
AK
AM
R
27
26
AF
R8
1K
+5V
C5
1000p
IC5
+5V
R9
2·2K
R10
·0K
OPEN I/P
GATES
E
VT1
C13
·01
0V
ME
CMD
13
13
C18
·01
R40
10M
R4
220
MR4
0V
+5V

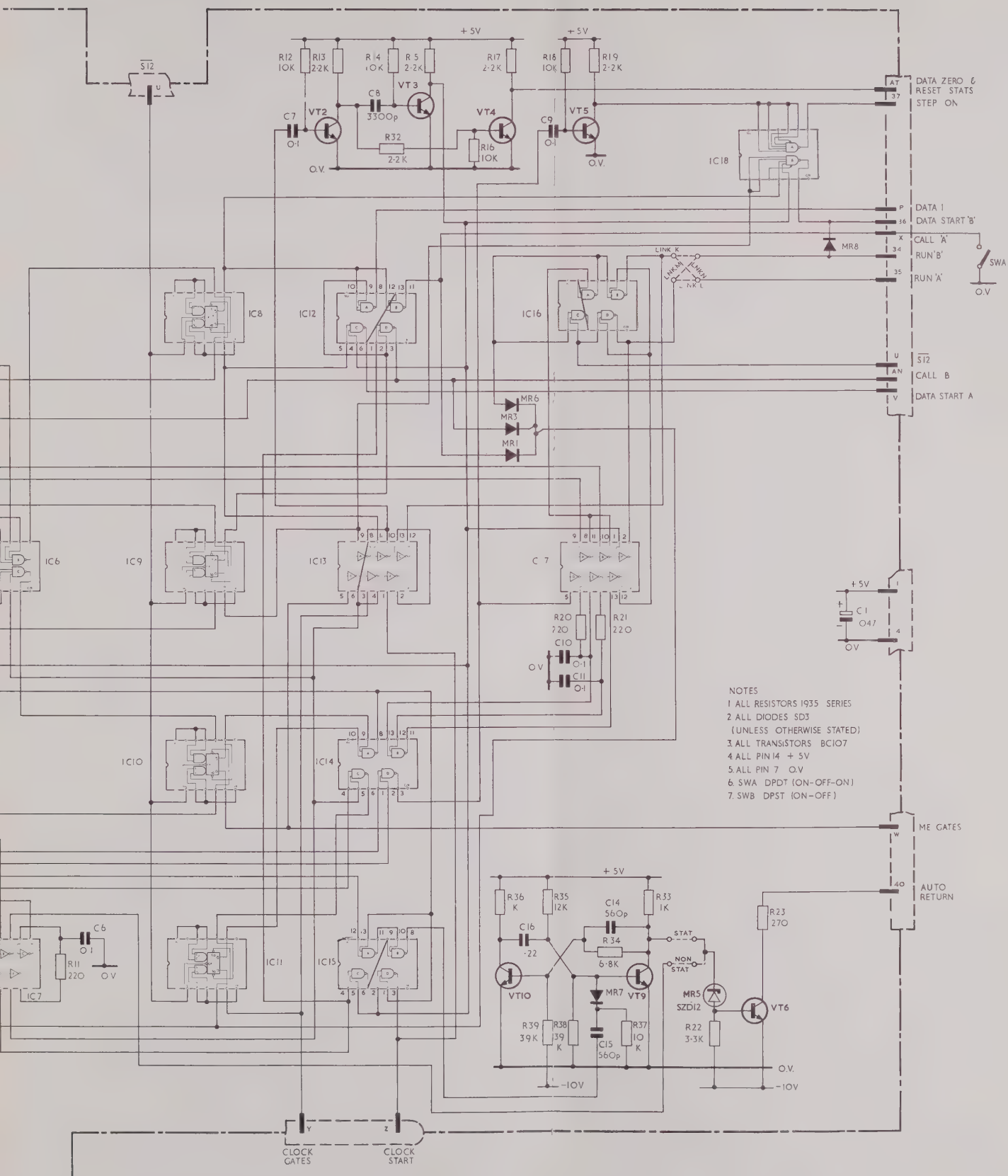
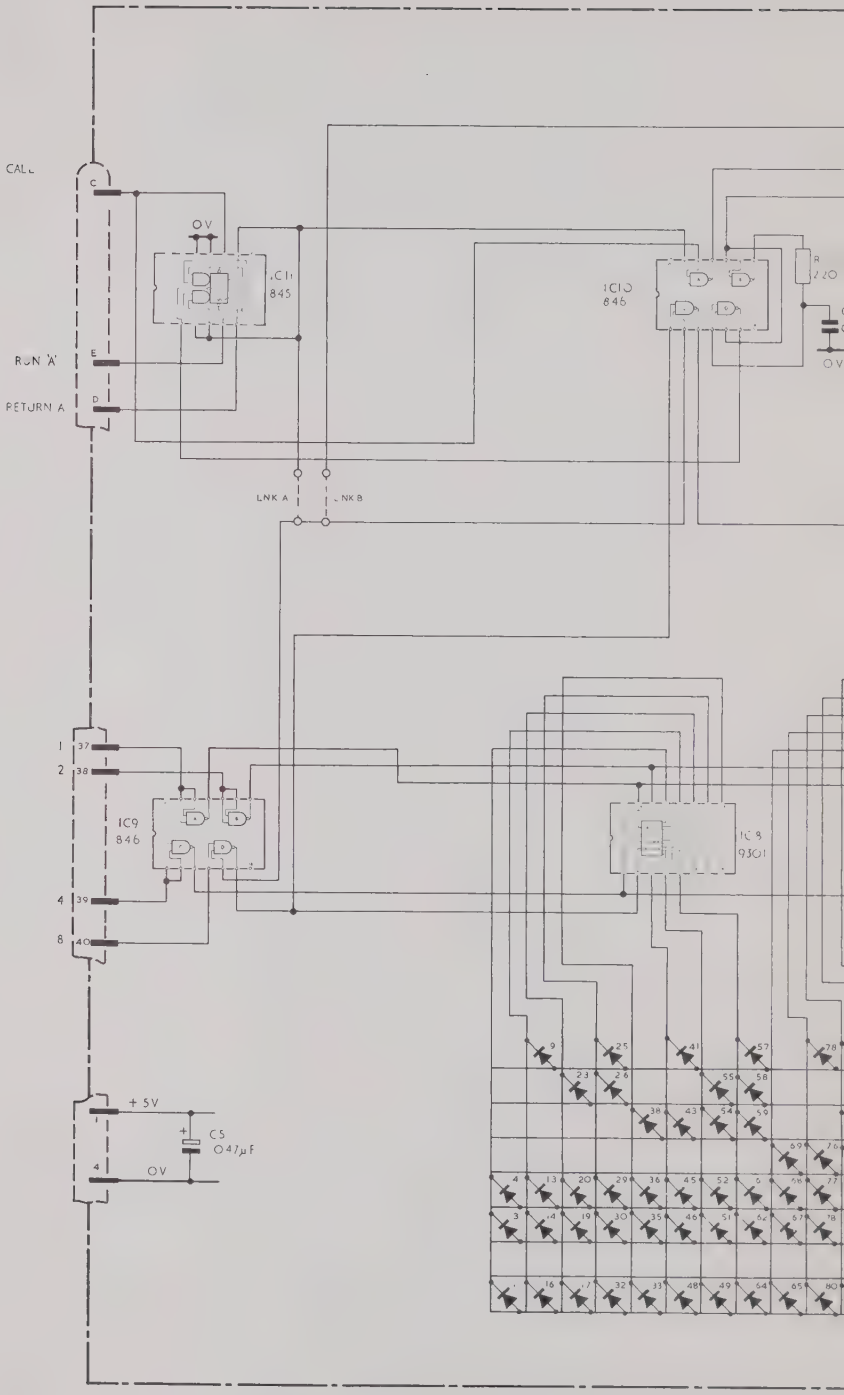


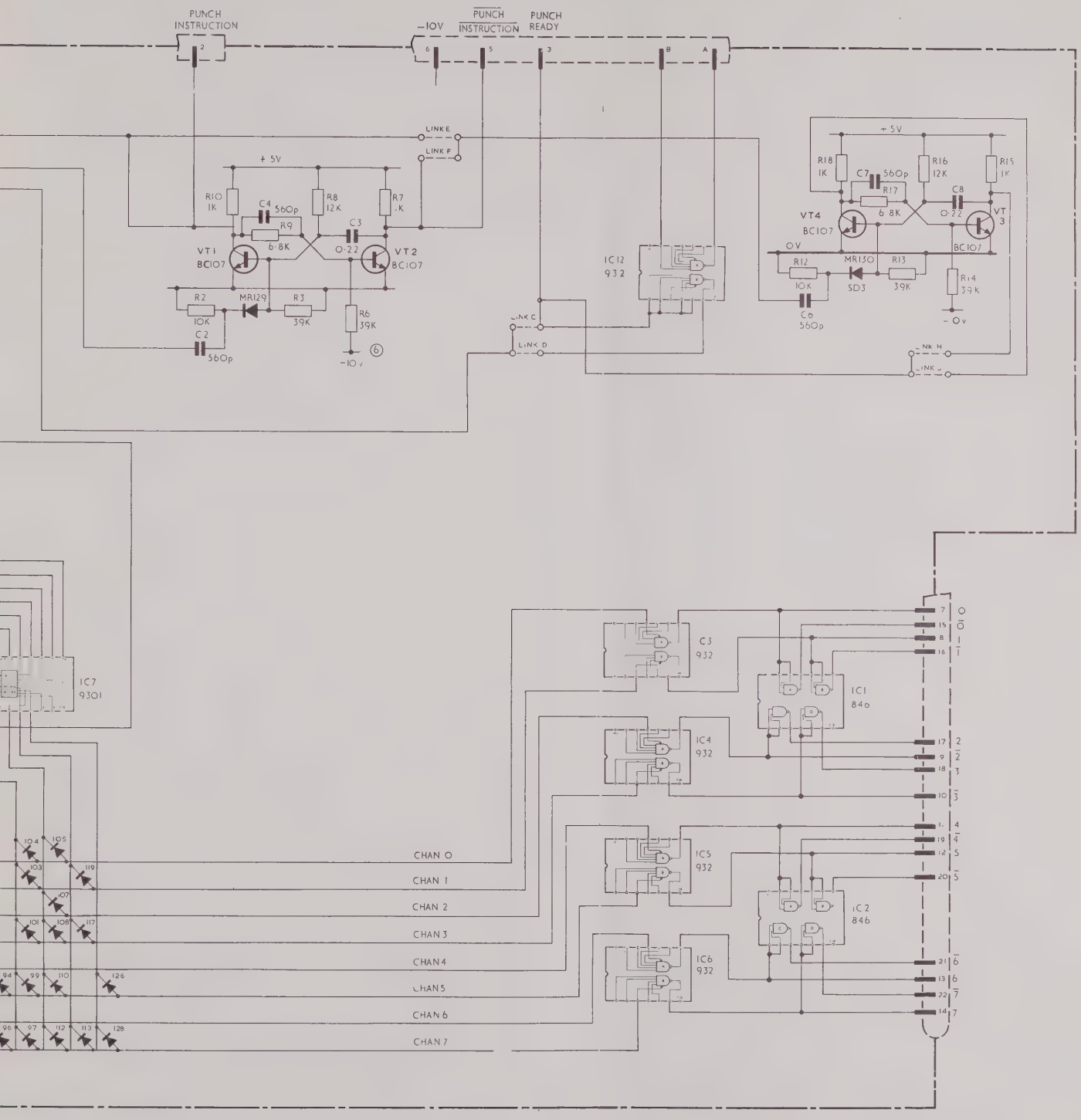
Figure 4.9 Serialiser Logic Circuit Diagram D1972930-4



NOTES

ALL ICS

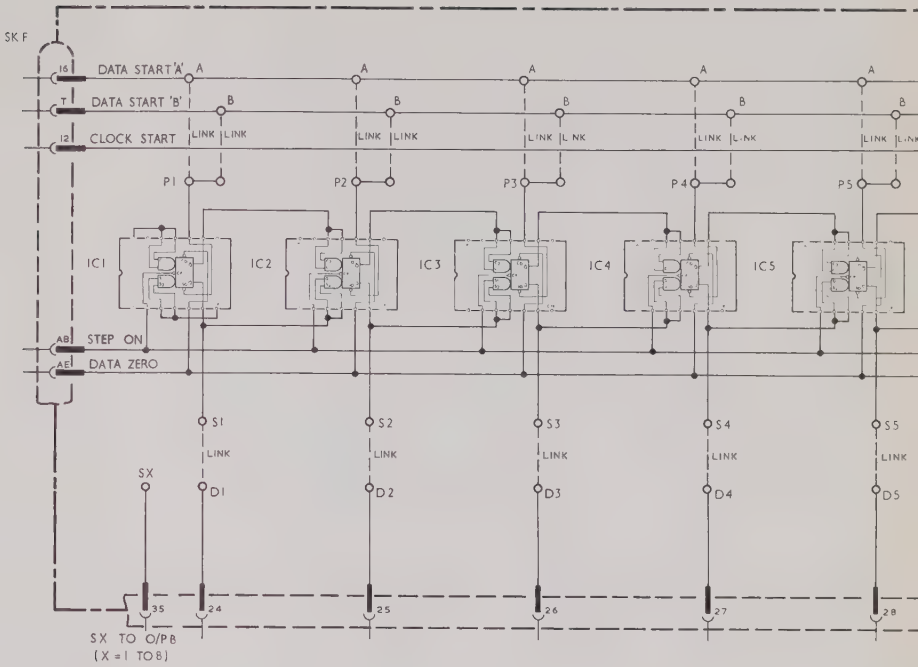
1. ALL DIODES SD3
2. PIN 14 + 5V, EXCEPT FOR IC9301 WHERE PIN 16 + 5V
3. PIN 7 0V (EXCEPT FOR IC9301 WHERE PIN 8 = 0V)
4.
5. LINKS A & C NORMALLY MADE

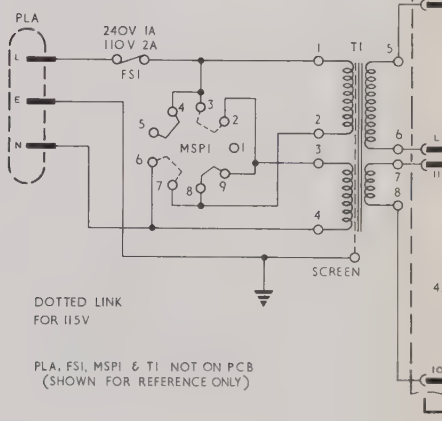


A 130·6 69

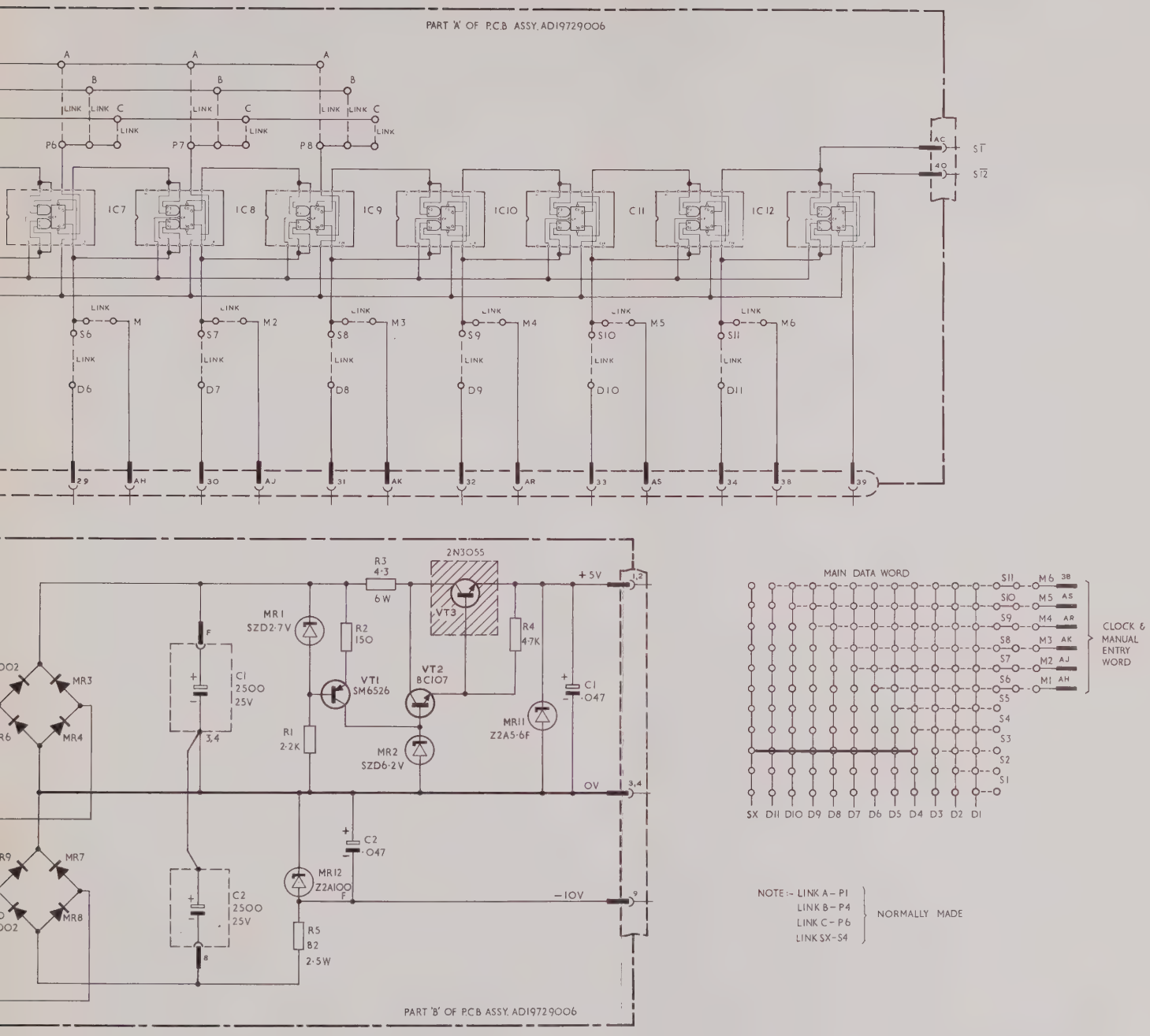
Figure 4.10 Decode/Encode Circuit Diagram

D1972930S



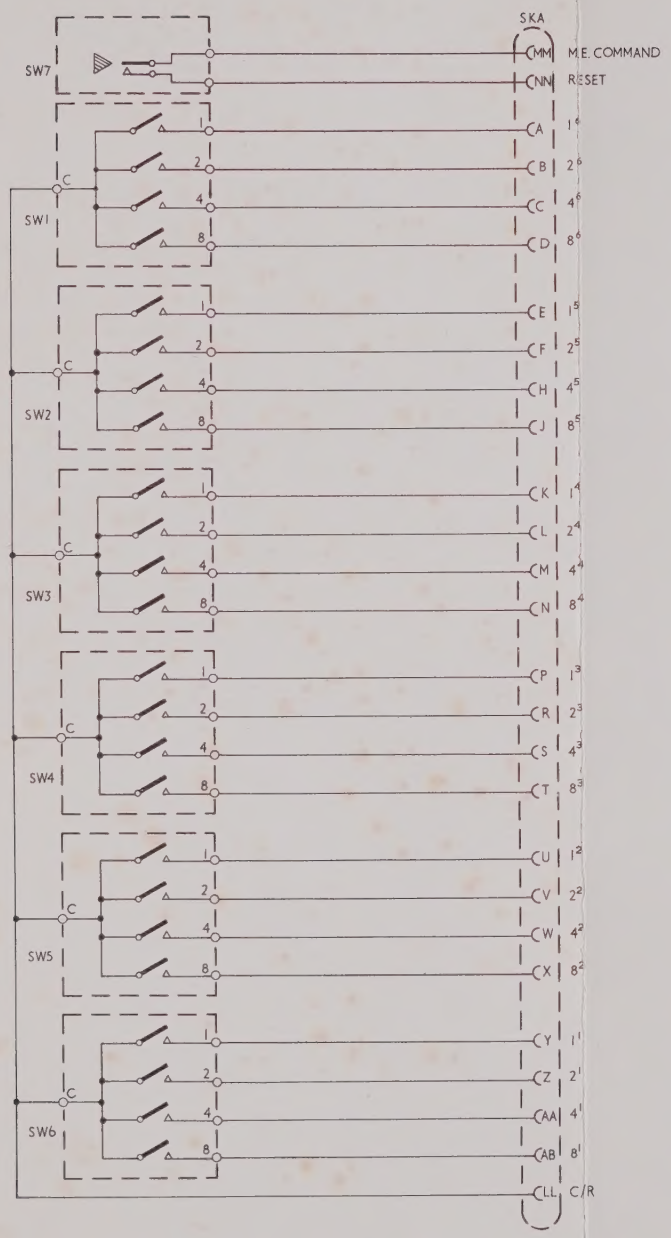


NOTE
1 ALL BISTABLES IC1 TO IC12 SN15845N
2 ALL COMP OUTSIDE BOARD PERIMETER
LINE NOT ON P.C.B & ARE FOR REF ONLY
3. IC'S PIN 7 0V
IC'S PIN 14 +5V



B 28 B 69

Figure 4.11 Power Supply and Shift Register Circuit Diagram D19729306



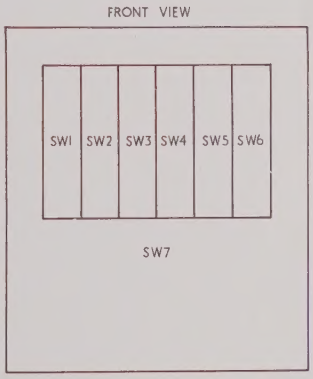


Figure 4.12 Manual Entry LU1960 Circuit Diagram C 19609301

MP MASTER
MA24422